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COMMENT

Last year was a busy one for technology and 2018 is unlikely to be any different

NEWS

Iron and oxygen hold the prospect of high capacity lithium batteries for a range of applications

Silicon anode project brings together partners looking to extend EV range

We take a look at a few of the most popular items on the New Electronics website during 2017

As the Cadence Academic Network celebrates its 10th anniversary, Patrick Haspel talks about future plans

INTERVIEW

A winning team
Digi-Key’s president and COO says that, whoever you’re competing against, you can’t be afraid of competition, adding the distributor’s culture is a winning differentiator

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A tipping point?
The Telecommunications Infrastructure Project is looking to apply open source technologies to address the challenges faced by next generation fixed and mobile networks

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Creating the right image
While machine vision systems historically relied on CCD image sensors, CMOS based devices have jumped to the forefront for many applications

START UPS

Driving innovation
Oxford University Innovation continues to impress, with a growing list of spin out formations, including Bodle Technologies and Metaboards. Why is Oxford so successful?

DIGITAL DESIGN

Careless whispers
Timing, EMI and even sound can provide attackers with information about the secrets held by a supposedly secure system. Countering threats requires vigilance and more careful digital design

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Ensuring software quality
As the software component in new products booms, how can companies ensure code quality when they are faced by time-to-market challenges?

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The next wave in timing innovation
Serdes reference clock performance is becoming increasing important as a range of networks move to higher data rates to support booming demand for bandwidth

MISSION STATEMENT

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COMMENT  TRENDS IN 2018

Tech trends
LAST YEAR WAS A BUSY ONE FOR TECHNOLOGY AND 2018 IS UNLIKELY TO BE ANY DIFFERENT.

It looks like 2018 will continue in much the same way that 2017 did – and that means it’s going to be busy. So, what are some of the key trends that are likely to be affecting the way we interact with and use technology in the coming twelve months?

One thing is certain; the increased ‘datafication’ of peoples’ lives will continue apace and that’s not really a surprise when you consider that almost everything we do leaves a trail of data. The amount of data being generated is doubling every two years and 2018 won’t see a change in that. Feeding this growth in data is the IoT, which is reaching further into our world – from cars to smart TVs and everything in between.

How we interact with technology is also likely to change as the adoption of voice technology accelerates. Building on the success of devices from Amazon, Apple and Google, it is estimated that, by 2020, 50% of all searches will be by voice and some 30% will involve no screen whatsoever. So could we start to see devices like Amazon’s Alexa or Google’s Home starting to ‘talk back’?

AI and automation began to dominate public debate in 2017. As machines become more intelligent, they’ll be able to do more things. The debate about the impact this will have in terms of processes, decisions, functions and systems will intensify as humans will no longer be needed to do the jobs that machines will be able to do faster, more safely, cheaper and more accurately.

Expect cybersecurity to continue to dominate the news. What had been considered to be in the realm of science fiction by many – just consider the WannaCry attack in May – is now becoming a scary reality.

For many, 2017 was an *annus horribilis* for the technology industry, with a growing number of companies accused of putting growth ahead of social responsibility and providing a platform for misinformation. As a result, it is likely that calls for much greater industry transparency will grow.

It’s going to be an interesting year.

Neil Tyler, Editor (neil.tyler@markallengroup.com)
UV-B comms system transmits 71Mbit/s

Researchers at the King Abdullah University of Science and Technology have demonstrated data transfer using UV-B light. The team used an LED to send pulsed UV-B signals to a sensor comprising two antireflective lenses that focused UV-B light onto a photodetector. The team observed strong power transmission, even when the angle between source and detector was increased up to 12°, demonstrating that direct line-of-sight was not required. The system transmitted data at 71Mbit/s.

Temperature dependent conductivity

A research group at the University of Bayreuth has controlled temperature dependent thermal conductivity with the help of photonic crystals. The findings are likely to lead to new thermal insulation concepts.

Photonic crystals have mainly been investigated for their optical effects. However, Professor Dr Markus Retsch said his team has developed four ways to control temperature dependent heat transfer in such crystals. “The findings demonstrate that it is possible, in principle, to regulate thermal conductivity in nanostructured materials with a high degree of precision,” said Prof Retsch. “In the long term, these concepts could be valuable for the development of thermal transistors or diodes.”

Altium launches Designer 18

Looking to address the changing requirements of engineers, Altium has released Designer 18. The upgrade provides an enhanced user interface and updates that work together to deliver a more cohesive design environment.

In addition to a redesigned user interface, version 18 features an upgrade to a 64bit architecture, combined with multi-threaded task optimisations, enabling users to design more complex boards more quickly.

An update to ActiveRoute supports length tuning, pin-swapping and gloss options, while the ActiveBoM editor has also been enhanced with a rule checker that allows users to verify each BoM line item. Additionally, multiboard assembly capability enables real-time connection management.

Iron could bring better batteries

IRON AND OXYGEN HOLD THE PROSPECT OF HIGH CAPACITY LITHIUM BATTERIES. GRAHAM PITCHER REPORTS.

A battery developed by researchers from Northwestern University and the US Argonne National Laboratory uses iron and oxygen to provide a high capacity device with multiple applications.

According to the team, the rechargeable lithium-iron-oxide battery can cycle more lithium ions than its lithium-cobalt-oxide counterpart. Lead researcher Professor Christopher Wolverton said: “The fact that it actually works is remarkable.”

The team noted that iron has not been applied successfully in batteries to date and the fact that oxygen is used to help drive the chemical reaction was expected to cause the battery to become unstable.

Using computational calculations, the team discovered the right balance of lithium, iron, and oxygen ions to allow the oxygen and iron to simultaneously drive a reversible reaction without allowing oxygen to escape.

“Not only does the battery have an interesting chemistry – because we’re getting electrons from both the metal and oxygen – but we’re using iron,” said Prof Wolverton. “That has the potential to make a better battery that is also cheap.”

Importantly, the battery – said to be fully rechargeable – starts with four lithium ions, instead of one and the opportunity to cycle all four back and forth by using both iron and oxygen to drive the reaction is described by Prof Wolverton as ‘tantalising’. “Four lithium ions for each metal – that would change everything,” he concluded.

Eel inspires new battery

The electric eel has inspired an international research team to develop a novel power source and suggest its work could enable self-powered batteries for biological applications such as pacemakers.

The researchers began by reverse-engineering the eel’s electric organ – made of electrocytes. These generate a small voltage through the movement of sodium and potassium ions. Together, these cells can generate up to 600V.

The team, led by University of Fribourg Professor Michael Mayer, designed a power source that generates electricity based on the salinity difference between compartments of fresh and salt water. By arranging hundreds of these compartments in a repeat sequence, it was possible to generate 110V. Each component is made of a hydrogel that can be assembled on clear plastic sheets using a 3D printer.

Two qubit silicon gate created

Researchers at Princeton University have constructed silicon hardware that can control quantum behaviour between two electrons with extremely high precision.

The team constructed a two qubit gate that controls interactions between the electrons in a way that allows them to act as the qubits necessary for quantum computing. The demonstration of the gate is being seen as an early step in building a more complex quantum computing device from silicon.

The gate was constructed by layering aluminium wires onto a highly ordered silicon crystal. The wires deliver voltages that trap two single electrons, separated by an energy barrier, in a double quantum dot.

By temporarily lowering the energy barrier, electrons can entangle and be used as qubits.

9 January 2018   www.newelecronics.co.uk
Silicon anodes to push EV range

SILICON ANODE PROJECT SEeks TO EXTEND EV RANGE. GRAHAM PITCHER REPORTS.

A £7million award from Innovate UK as part of the Faraday Battery Challenge is funding a project to develop significantly better materials for Li-ion batteries. The work, featuring silicon anode pioneer Nexeon, is described as an essential step towards enabling electric vehicles (EVs) to have a range of more than 400 miles.

The SUNRISE project is looking to develop better battery materials based on silicon as a replacement for carbon in the cell anode, and to optimise cell designs for automotive applications.

Nexeon will lead the silicon material development and scale-up stages of the project, while polymer specialist Synthomer will lead the development of a next generation polymer binder optimised to work with silicon and to ensure anode/binder cohesion during a lifetime of charges. Meanwhile, Nexeon and UCL will lead material characterisation and cell performance work.

“The biggest problems facing EVs are almost all related to limitations of the batteries,” said Nexeon’s CEO Dr Scott Brown. “Silicon anodes are now well established on the technology road maps of major automotive OEMs and cell makers, and Nexeon has received support from UK and global OEMs, several of whom will be involved in this project as it develops.”

The Faraday Battery Challenge, announced in July 2017, will see £246m invested over four years to ensure the UK leads the world in the design, development and manufacture of batteries for EVs.

Direct metal printing

North Carolina State University researchers say a technique they have developed for directly printing metal circuits could enable the creation of flexible and stretchable electronics. The technique, which can use multiple metals and substrates, is claimed to be compatible with existing manufacturing systems that apply direct printing technologies. However, ink is substituted with molten metal alloys with melting points as low as 60°C. So far, the team has printed three alloys on glass, paper and stretchable polymers.

A further benefit is the circuits may be capable of ‘healing’ themselves if broken or stretched too far.

Graphene in space

In a collaboration between the Graphene Flagship and the European Space Agency, experiments have tested the use of graphene in space-related applications.

“Graphene, as we know, has a lot of opportunities. One, recognised early on, is space applications and this is the first time that graphene has been tested in space-like applications,” said Professor Andrea Ferrari, the Flagship’s science and technology officer.

Graphene shows promise for use in loop heat pipes and could also be used in propulsion, due to its lightness and strong interaction with light. Both applications have been tested recently.

The main element of the loop heat pipe is a metallic wick, where heat is transferred from a hot object into a fluid, which cools the system. Wicks made from two types of graphene were tested in two ESA parabolic flights and the results have encouraged the Flagship to push towards a commercial product. Meanwhile, five experiments demonstrated laser-induced motion of a graphene light sail.

‘Complete’ quantum chip design

A team from the University of New South Wales says it has created a complete design for a quantum computer chip and adds the device can be made using mostly standard industry CMOS processes and components.

Showing confidence in its work, the team has struck a $83million deal to develop a 10 qubit prototype silicon quantum chip by 2022.

Researcher Dr Menno Veldhorst said: “It’s generally accepted we will need millions of qubits working in tandem. To do that, we will need to pack qubits together and integrate them, like we do with modern microprocessors.

“Our design incorporates conventional silicon transistor switches to ‘turn on’ operations between qubits in a vast 2D array using a grid-based ‘word’ and ‘bit’ select protocol similar to that used in a conventional memory.

“By selecting electrodes above a qubit, we can control a qubit’s spin. And by selecting electrodes between the qubits, two-qubit logic interactions, or calculations, can be performed.”

Ultra low power MCU

French IP developer eVaderis has worked with Beyond Semiconductor to create what is said to be a fully functional ultra low power MCU featuring on-chip MRAM. The test chip, based on Beyond’s BA2X product line, is said to be suitable for use in battery powered IoT applications, including wearables.

The test chip, made on Globalfoundries’ 40nm low power CMOS process, features 3Mbit of STT-MRAM distributed across the design, addressing such functions as working memory, configuration, state retention, code execution and data storage.

“Power consumption is still the key challenge for any battery-powered device,” said Matjaz Breskvar, Beyond’s CEO. “We have been working with eVaderis to jointly realise a vision of battery-powered, always-on devices with unprecedented energy efficiencies.”
A New Year has arrived and we can expect to see a host of new and exciting innovations. But 2017 also saw a number of stand out news stories and product launches.

Top news
The world is gradually becoming wireless and following this trend, 2017 saw the introduction of a device that could charge a moving object wirelessly. Developed by Stanford University scientists, this new technology can be used to charge electric cars on the motorway, medical implants and cell phones, as the car or individual passes by. This gadget, which could remove the need to stop and recharge, proved to be of particular interest to readers.

A MEMS microphone that enabled voice activation, while drawing almost no power came a close second in our most-read news. Vesper, an acoustic sensor developer, launched the VM1010. The first of its kind, it is said to allow product designers to offer touchless user interfaces without power consumption penalties.

Voice enabled devices was a popular topic last year. XMOS launched the XVF3000 family of voice processors. The parts are said to enable voice capture at distances of 5m or more via arrays of MEMS microphones.

Top feature
There was a keen interest in battery life in 2017, and the feature on the potential breakthroughs in battery technology received an extraordinary number of reads.

Ilika, which has been developing new materials for energy and electronics applications for more than a decade, has developed an innovative solid state battery technology for a range of applications and is licensing the IP for use in a variety of end user markets.

Graeme Purdy is chief executive, said: “There’s a wide range of cathode and anode materials which give different performances and which can be optimised for applications such as safety and capacity. And the voltage at which these cells operate can be tuned, as can the cycle life.”

However, it’s the next generation of battery technology on which Purdy and Ilika have their eyes focused, which Purdy explained may well be based on lithium.

Ilika is taking part in a three-year project led by Johnson Matthey to develop protected anodes for lithium sulphur batteries. Other partners include Williams Grand Prix Engineering, the University of Oxford and the University of Warwick.

However, the partners are not alone in this venture, Oxis Energy has been working on Li-S technology since 2004. It now has a patent portfolio covering electrolyte systems for Li-S cells, methods of Li-S cell construction and positive and negative electrodes.

While lithium remains the material of choice for batteries, researchers are looking at other elements such as sodium and magnesium based rechargeable batteries.

The second most popular feature online looked at building security into IoT devices.

IoT devices, which transmit and receive data and commands over the world’s universal network, are exposed to a far greater variety and number of threats than earlier products that supported machine-to-machine (M2M) communication, typically over a closed, private network.

The STRIDE threat classification model, originally developed by Microsoft, lists the potential security threats an IoT device or user of that device faces: Spoofing; Tampering; Repudiation; Information disclosure; Denial of service; and Elevation of privilege.

Jack Ogawa, senior director of marketing at Cypress Semiconductor, explained that the new demands generated by the IoT, call for new MCUs that are purpose-built for the IoT with their own security features, low-power attributes and processing capabilities.

Products
Last year also saw a number of interesting product releases. One of the most read on New Electronics online was created by SST Sensing and Sparkfun. The pairing saw the development of a simple to implement liquid level switch using infrared technology. This comprised an Optomax Digital liquid level switch which is connected to an Arduino board via the TTL output and powered by a 5V source.

There was a lot of interest in a real-time Ethernet multi-protocol switch chip from Analog Devices supporting time sensitive networking. Called fido5000, the part is said to reduce board size and power consumption while improving Ethernet performance at the node under any network load condition. Potential applications include connected motion systems, such as robotics, and intelligent factories.

Last, but not least, on our top-read list, was the news that KiCad’s open source EDA software had been added to Digi-Key’s list of EDA model output formats for schematic symbols and PCB footprints.

Using the tools, customers can verify the Digi-Key and manufacturer’s part number, preview graphics for the models, choose the output formats, and download up to 15 parts per month.
The Cadence Academic Network has celebrated its tenth anniversary. Started by Patrick Haspel in 2007, it was, initially, purely a European exercise but now encompasses both the US and Asia.

“The academic network is not a standard university programme,” Haspel explains, “but rather a marriage between industry and academia that is unique in the semiconductor ecosystem. It’s about developing long-term relationships with academia embracing both professors and students.

“It is an essential part of our commitment to help develop the next generation of engineers as we reach out to key universities to ensure better understanding of electronic design automation.”

The network came out of Haspel’s experiences as an academic at Universität Mannheim, when he was asked to create a digital design lecture series.

“While I wanted to pull together a single flow, that proved impossible; no one from the EDA space wanted to talk or share their tools with a university at the time,” he recalls.

As a result, he created and set up his own network at the university and established the first ASIC competence centre.

“It wasn’t until 2002 that I met with Cadence and we got access to their tools,” he remembers.

Haspel went on to join Cadence in 2005 and in 2007 formally introduced the Cadence Academic Network, which was intended to help universities get access to EDA tools and ideas.

“From my experience, there was a need for a more sophisticated design flow, or EDA environment, at university and I thought academia would really benefit from a closer relationship with the EDA vendors.

“The Network originally started as a pilot programme in central Europe and was then rolled out across EMEA,” Haspel explains. “Then around three years ago, it was introduced into the other regions.”

The academic network encourages the correct use of EDA software by universities, as well as connecting professors and academics.

“But it also lets Cadence tap into the research competencies and interests of the universities,” he says.

“Initially, academics didn’t realise the value of events such as CDNLive, where they could exchange ideas and network – it wasn’t perceived as a scientific event. Once they began to engage, it became easier and we’ve seen a massive increase in research submissions.

“Only a few universities are using EDA to provide tape-outs, many simply use Cadence technology as part of their courses.”

Crucially, students benefit as they get to spend more time on their research than wasting time looking for EDA tools.

“The Network has helped to improve the perception of the Cadence brand. We’re presenting at conferences, and sponsoring academic events. It’s a remarkably stable partnership between industry and academia in which we share and exchange knowledge, tools, and students,” enthuses Haspel.

Over the years, Cadence has developed a strong relationship with academia, even though there is no cash contribution from Cadence.

“It has made a real difference for the company,” according to Haspel.

“Education in advanced verification is a new field, few academics actually teach it. We can help improve teaching material which, in turn, will help us to sell our technology.”

Part of Cadence’s mission is to also help commercialise academic research.

“The challenge is finding ways to build pathways to commercial use.”

With a growing number of spinouts from universities, the Network can play an important role providing a bridge between academia and the commercial world.

“We want to extend the Network further,” Haspel says, “but it will take time.”

With the advent of new technologies there will certainly be a need for closer research collaboration, “and that will drive a need for much greater levels of engagement.”

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**News Analysis: Academia Network**

**The Cadence Academic Network is 10 years old. Patrick Haspel, who set up and runs the programme, talks to Neil Tyler about future plans.**

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It’s now more than two years since Mark Larson stepped down as president and chief operating officer at Digi-Key, the electronics components distributor.

“Mark was certainly a visionary, who led the company from 14 employees to one that now employs more than 3400 globally,” says Dave Doherty, the company’s current president and COO. “He had a vision and almost single-handedly pushed the business forward, turning it into an organisation with an annual turnover in excess of $2billion.”

Doherty had been with the company for many years before his appointment in 2015, having served as the company’s executive vice president of operations.

“When I was appointed as Mark’s successor, I realised that the business had become too large and complex for one person to manage and would require a management team capable of communicating in an open and transparent way, if we were going to deliver business improvements going forward,” Doherty explains.

“We took the role that Mark had, and while I assumed some of that, we sought to diffuse other elements of his responsibilities out across the broader team,” he says. “There’s a real sense of camaraderie here and decisions can be made quickly, which means that we can experiment and be flexible.

“Crucially, we’re open to honest and constructive criticism. Collective decision making is also about respecting what’s been built, and acknowledging the success that’s been achieved and embracing the culture that’s developed over the years.”

It’s that culture, one of service and hard work, that Doherty believes sets Digi-Key apart from its competitors.

“It’s not the processes we use or the logistics companies we employ, but the people who work here,” Doherty argues. “That’s the key differentiator. I’m not from this region – Minnesota – but I’ve never seen people so committed to a company.

“Digi-Key is part of the local community and there’s a real sense of pride about the work people do.

“The culture here can be described as ‘we don’t leave until the job is done’ and that’s true of everyone, whether they work in the warehouse or are part of the management team.”

The importance attached to the workforce suggests that one of Digi-Key’s biggest challenges is recruitment.

“With more than 90% of our workers living locally in Thief River Falls, it’s a challenge,” concedes Doherty.

“A few years ago, we struggled with churn. We’d brought in external advisors to help manage the business and had been running a policy of mandatory overtime. In the process, we lost the hearts and minds of the people who work here. And that was certainly a ‘stumble’ on our part.

“Deep down, our employees see themselves as stakeholders in the company’s success and I think we forgot that. Today, we no longer have mandatory overtime. While overtime is available – and when we’re processing as many as 21,000 orders a day – it’s vital, we offer our staff much greater flexibility. We appreciate that they have to manage commitments external to the business.

“As a result, we’re seeing more people volunteering for overtime and we have people from all functions of the business working in the warehouse. One of the benefits of that is that they get to understand each other roles better.”

Doherty can often be found working in the warehouse and engaging directly with the workforce.

“Training has an important role to play and is a crucial part of our commitment to the workforce,” explains Doherty, “especially as we look to expand the business and embrace automation. We need to empower our people to make those changes work.”

Looking to the future

Digi-Key is looking to expand its facilities and having acquired a large tract of land next to the current building, is set to ‘break ground’ in the Spring.

“It’s a significant investment on our part,” concedes Doherty, “and while we do have a facility in Fargo, which is around 100 miles away, we wanted to bring as much as we could onto the one campus.

“We’ll look to move professional functions to the new facility, which will free up space in the existing building. Fargo provides us with 400,000sq ft and will be used as a repository for extra inventory, but we will also look to use it to develop new business concepts and ideas.”

The expanded facility at Thief River Falls will provide Digi-Key with three times the current usable space and is expected to be ‘up and
running’ within the next three years. According to Doherty, the facility will embrace new digital technologies, including automation and artificial intelligence (AI).

While he is reticent to discuss the company’s plans for AI, he accepts that automation will have a significant impact.

“Automation will impact on our rate of hire,” he notes. “We employ more than 3000 local people – that’s a third of the county that works here. We’ve recruited more than 1800 people in the past 10 years and we are looking to take on a further 1000 in the coming 10 years.

“We understand that we have a community role to play. When we first looked at investing in new facilities, we were advised to look at moving to a big regional hub, but none of us were comfortable with that idea and, to be honest, I don’t think, with our service model, that location is a significant issue.

“Looking to the future, automation will impact on fulfilment but we’ll need to employ people to work in customer services, IT, engineering, marketing and accounting as the business grows.”

When asked about the company’s plans to use AI, Doherty’s response is ‘stay tuned’, but it’s clear it is set to invest heavily in new technologies.

“Digital transformation is expensive, but a number of initiatives are under way,” he says.

All this investment comes at a time when the company is seeing double digit growth, well in excess of the industry average.

“Growth is being driven by innovation across all our main markets. Innovation never dies. Engineers require access to broad product lines and look for reliable and fast delivery of orders and that’s what we do. We have more than 650 lines in stock and have responded to changing customer requirements by adding more than 89 new suppliers in the past 12 months alone.

“The competitive nature of the market is changing and forecasting customer demand remains problematic. History is often said to be the best predictor of the future, but I don’t think that’s as true as it was, but the opportunities for us going forward are certainly huge.”

As a private company, Digi-Key can respond quickly to new competitive threats; whether from existing competitors or from new entrants into the market, such as Amazon.

“Whoever you’re competing with, you can’t be afraid of competition,” Doherty concludes. “I’m not naïve about the competitive threats we face, but teams that win tend to be those that play for one another and I believe that what we have created here at Digi-Key is unique.”
The Telecom Infra Project (TIP), conceived by Facebook to light a fire under the traditional telecommunications infrastructure market, continues to expand into new areas.

Launched at the 2016 Mobile World Congress in Barcelona, the highly disruptive project takes an open ecosystem approach to foster network innovation and improve the cost efficiencies of both equipment suppliers and network operators.

“We know from our experience with the Open Compute Project that the best way to accelerate the pace of innovation is for companies to collaborate and work in the open. We helped to found TIP with the same goal – bringing different parties together to strengthen and improve efficiencies in the telecom industry,” according to Aaron Bernstein, Facebook’s director of connectivity ecosystem programmes.

The project was launched by Facebook, SK Telecom, Intel, Nokia and Deutsche Telekom with the aim of improving global connectivity, notably in areas that currently lack access to the internet or to mobile networks.

BT, Vodafone and Telefonica soon joined the party and all now have representation on the TIP board.

Conspicuous by their absence are the big US mobile operators and the likes of Ericsson and Huawei.

The group boasts 500 members, and last November’s second annual TIP summit in Santa Clara drew 1200 attendees, 400 more than the previous year.

“Unfortunately, the number of active members contributing to research and development in a meaningful way is more like 100, with, let’s say, 80% of members simply monitoring progress,” said Axel Clauberg, VP of transport, aggregation and IP at Deutsche Telekom and current TIP chairman. “Such a transformative project takes time to embed. Look at Facebook’s previous initiative in the area – the Open Compute Project. That took some five years to gain real traction.”

The TIP is not just an altruistic initiative on Facebook’s part. At its core, it is trying to solve a problem partly created by the company, which depends hugely on the ability of network operators to keep pace with explosive growth in demand for bandwidth.

Neither is it a coincidence that the projects underway include collaboration into areas such as open-source based long distance antennas that will help bring internet to remote locations and the development of tiny cellular base stations that could be planted on street lighting to speed deployment of wireless services.

Clauberg pointed to another reason why operators are keen on the TIP approach. “[It’s] one of the ways we could and must improve on capital efficiency. We are seeing massive growth in data traffic, yet are struggling with flat average revenues per user in many markets.

“We need more radical and disruptive approaches to improve the way in which we develop and implement existing infrastructure, while maintaining good relationships with our existing suppliers.”

The TIP chairman also pointed to another stark reality for network operators and, to a lesser extent their suppliers. “The best, brightest people leaving colleges and universities want to work for the big and increasingly influential web companies, such as Facebook, Google and Amazon, or do their own thing. We are struggling to attract the talent that, for decades, we took for granted.”

Interestingly, the large US carriers
more to the cost of getting electricity to remote base stations and finding concrete roads to help erect the necessary towers and accompanying infrastructure. This is misleading; minor improvements in the cost of electronics in infrastructure gear will not make a big difference here.”

**Criticism of the project**

Clauberg was assertive about criticism from some that the TIP project was undermining the industry’s standardisation efforts. “We are most definitely not replacing standards bodies and our work in no way undermines the strenuous efforts towards what we all believe is a hugely important issue – a good outcome to the efforts towards 5G standardisation.

“This is a critical challenge for the industry.”

Nor does the TIP chairman accept that ‘open source’ is an issue.

He suggested there seems to be some confusion between ‘openness’ – basically interoperability between infrastructure solutions offered by different vendors, but based on standard interfaces and APIs – and ‘open source’.

Clauberg stressed there is room for both approaches within the project and noted that two of the working groups follow the ‘royalty free’ approach. OpenCellular is targeting cheaper base stations, while the majority of members have opted for the RAND licensing approach – the so-called ‘reasonable and non-discriminatory’ licensing terms.

This, Clauberg continued, accurately reflects the IPR reality faced by the industry. “Start-ups wishing to join or who have been chosen to work within the group should not be worrying about their intellectual property rights.”

Another criticism of the TIP is that there are just too many projects and that it would be better to focus on some key issues facing the sector.

The TIP board clearly rebuffed this at last November’s TIP Summit, where a number of innovative work groups were launched. One of these, led by BT, focuses on end-to-end network slicing – the concept of automatically provisioning a cross-domain data pipe that specifically targets the requirements of a particular service, whether that is low-capacity, intermittent IoT use or high capacity, latency sensitive. The work should be particularly relevant to forthcoming network architectures, Clauberg contended.

The TIP chairman also said the important mmWave Networks project group, co-chaired by Deutsche Telekom with Facebook, now has 200 members, including chip-set makers, operators, backhaul network vendors, system integrators and test and measurement companies.

The target is to make mmWave a complementary broadband option to fibre and the group will focus its efforts on the 60GHz band, which can support the bandwidth required by almost all current and emerging applications, such as 4K video streaming and smart sensors.

The group is building on some of the data and lessons gleaned by Facebook from its Terragraph project. This involved building and running field trials of a 60GHz multi-node wireless system that it said overcame the signal range and absorption limitations that have, to date, confined this frequency band to indoor use.

Bernstein pointed to progress by the OpenCellular project in developing cost-effective and sustainable base stations that are now undergoing lab and field trials with an all open source platform. “Vodafone, MTN and Telefonica are among the leading operators looking to use OpenCellular to potentially serve millions in small rural towns and villages that lack network coverage,” he said.

The LTE eNodeB reference design is provided by Cavium, while NuRAN Wireless designed the 1800MHz front-end. Facebook and Keysight - such as Verizon, AT&T and Sprint – have not joined the initiative as yet and the only big North American carrier on board is BCE (Bell Canada), alongside some mid-size cable networks, such as CableLabs and Equinix.

There are also some glaring omissions on the infrastructure equipment side. While Nokia is a founding member, it has contributed little to the development work and Ericsson has yet to sign up.

“Facebook is giving the impression that telecoms infrastructure is expensive today and that its approach will lower costs. We disagree,” suggested Martin Bäckström, head of technology and portfolio in Ericsson’s business area. “Our and other suppliers’ gear still offers an excellent return on investment for the operators.

“They are also pushing the idea that the project is targeting better connectivity in emerging markets and in remote areas. Having worked for many years at a major operator in The Philippines, the real problems relate

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**“We need more radical and disruptive approaches to improve the way in which we develop and implement existing infrastructure.”**

Axel Clauberg

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Another new initiative is the Artificial Intelligence and Machine Learning group, co-chaired by Deutsche Telekon and Telefonica. Amongst the projects planned for this group are: techniques that can spot and predict network outages; network planning routines that will help operators put cell towers in optimal locations; and an exploration of how latency-critical services, such as autonomous vehicles, can be refined by predicting customer behaviour.

Perhaps the most important and concrete success of the TIP to date has been the development of Voyager within the Open Optical Packet Transport (OOPT) group. The white box DWDM transponder and router is now going through the final stages of engineering and, according to Clauberg, continues to gain momentum worldwide.

The operators say such technology, meeting challenging size, weight and power requirements, will be crucial in 5G infrastructure and device developments.

“Minor improvements in the cost of electronics in infrastructure gear will not make a big difference here.”

Martin Bäckström

**Telecommunications Infrastructure Project looks to generate a new wave of innovative start-ups**

One of the most important aspects of the Telecom Infra Project is the way it intends to get large organisations to work with, mentor and kick-start a new wave of infrastructure start-ups.

The key to achieving this is not only to ensure emerging companies have access to funding, but also to adapt their technologies for real operational requirements within a network infrastructure and to test these ideas. This is why the project has been establishing what it terms TIP Ecosystem Acceleration Centres (TEAC).

“We are excited about the level of VC participation. For example, in 2017, UK-based investors committed $170million towards the TEAC in the UK supported by BT, while $115m was committed by French VCs to bolster the French TEAC supported by Orange,” said Aaron Bernstein, Facebook’s director of connectivity ecosystem programmes. Bernstein stressed neither Facebook nor the hosting operators are planning to make equity investments in companies chosen to work within TEACs.

Currently, there are four TEACs. BT is using its R&D facilities at Adastral Park and, to some extent, its operation at London’s TechCity, while SK Telecom is hosting companies at its research group in Seoul. More recently, Deutsche Telekom has set up a TEAC in Bonn

BT was also the first to announce the winning

Howard Watson, CEO of BT Technology, Service and Operations, pictured: “It’s more important than ever that we seek expertise, not only from our home-grown talent and established partners, but also from newly created small businesses.”

The TEAC concept is augmented by TIP Community Labs that provide space and innovation support from operators targeting specific project groups. The first was established at Facebook’s Menlo Park facility, followed by one in Berlin hosted by Deutsche Telekom focusing on mmWave network projects. Another lab at SK Telecom in Seoul is targeting emerging testing technologies.

Last November, the initiative was expanded with labs in Rio de Janeiro, set up by TIM to support efforts within the Open Optical Packet Transport project group; in India, where Bharti Airtel will support a focus on technologies related to the vRAN Fronthaul project group; and in the US, where CableLabs will target virtualisation of the radio access network.

There are also plans to open a lab at Facebook’s London headquarters to support European based projects.
SMARC Computer on Modules

SMARC is the first COM standard to be built specifically for modern ARM-Cortex system on chips (SoCs), aiming to efficiently pass along ARM benefits such as low power consumption to COTS designs.

The new standard for ultra low-power COMs was developed specifically for new modules with ARM and SoC processors and is characterized by the extremely flat build of its form factor.

It uses a 314-pin connector that has a construction height of just 4.3 millimeters (the MXM 3.0) with an optimized ARM/SoC pin-out definition. This connection method allows robust and cost-effective designs that have an extremely thin construction height.

There are 4 modules available:

- **SMARC-FIMX7**
  - NXP i.MX 7 Cortex-A7 Solo 800Mhz and Dual Core 1GHz
  - 1GB (Dual) or 512MB (Solo)

- **SMARC-FIMX6**
  - Freescale i.MX6 Cortex-A9 Solo, Dual-Lite, Dual and Quad

- **SMARC-T335X**
  - TI Sitara AM3354 @660Mhz, 800Mhz or 1GHz

- **SMARC - T4370**
  - TI Sitara AM4378 @ 800mhz or 1Ghz
Creating the right image

CMOS image sensors have developed to the point where they can be used in most machine vision applications. By Max Cavazzana.

As manufacturing systems become more intelligent – perhaps as the concepts behind Industry 4.0 become adopted more broadly – the need for more capable vision systems has grown sharply.

Machine vision systems use images to gather information on a system or process and then make decisions based on the images captured. While such systems are dependent upon lighting and software, the camera – and the image sensor within it – is the key component in the overall operation of the system, as well as its ability to improve manufacturing quality or increase productivity.

At a high-level, a typical machine vision application involves some combination of basic measurement, counting or inspection functions. Objects may be assessed to confirm the number of objects present, to determine the number and size of features or their quality level.

So machine vision could be used to not only determine that the proper number of holes have been drilled into an item, but also to verify the spacing and shape of each hole. Similarly, the location of an object may be determined in order for it to be picked up by a robot arm or to determine whether a feature is in the correct place. Other functions include reading a barcode, performing character recognition or measuring the level of a fluid.

Each of these functions drives specific characteristics required for the final camera system and, ultimately, the image sensor required for the application. Understanding the minimum quality level of the image is paramount as this determines whether the computer system analysing the image can make an accurate measurement or reach the correct conclusion. This point is critical; other features, such as frame rate, power or size, will become secondary if the images captured are not of sufficient quality for analysis and use.

Historically, machine vision systems have required CCD image sensors because of their high image quality and performance. Today, however, CMOS image sensors have jumped to the forefront for many machine vision applications. Advances in CMOS pixel design have made the imaging quality available from this platform sufficient for a variety of different end uses.

Modern CMOS image sensor platforms, such as that used in ON Semiconductor’s PYTHON family, are based on a global shutter pixel design that enables the capture of moving objects without the introduction of motion artefacts. In-pixel correlated double sampling provides low readout noise, while on-chip fixed pattern noise correction helps preserve image quality. Combined with a 10-bit A/D converter and a dynamic range of 60dB, these features allow machine vision systems to leverage the intrinsic advantages of a CMOS platform in their operation.

With many machine vision applications looking to operate at ever higher speeds in order to increase productivity, image sensors must support high bandwidth readout. The output architecture of the CMOS platform enables this as additional digital outputs can be added to increase the available bandwidth.

For example, the use of up to 32 separate LVDS outputs enables high resolution PYTHON devices to realise bandwidths that exceed those of modern computer interfaces, including 10Gbit Ethernet or USB 3.1. The ability to output at up to
80frame/s from a 25Mpixel device is well beyond the capabilities of standard CCD designs.

The inherent flexibility available in CMOS output designs allows the frame rate to be further increased when operating in Region of Interest (ROI) mode, where only a portion of the image sensor array is read out. With proper design considerations, the speed increase when operating in this manner can scale by both the x and y dimensions of the ROI, enabling faster frame rates than can be realised when using a more standard CMOS output design, which only scales the x dimension. Consider the frame rates from the PYTHON 5000 image sensor compared to theoretical frame rates from a similar 5Mpixel sensor using a standard CMOS output. At full resolution, both designs would provide approximately 100frame/s, but when reading out a 1280 x 720 pixel ROI, the the PYTHON device’s frame rate increases to almost 600frame/s, while the standard output design would increase to only 300frame/s. This can be an important differentiator.

While high resolution can provide finer detail, this must be balanced by making sure that too much information is not captured, which would slow data processing. In addition to having the right number of pixels, they need to be in the appropriate aspect ratio for the application. For example, an aspect ratios of 1:1 is often used in pick and place applications to maximise image capture across the full field of view.

Different spectral sensitivities, such as colour, monochrome and extended near infrared (NIR), may also be required to optimise the imaging system for the application. In order to do this, a camera manufacturer will look for an integrated family of image sensor products that includes multiple resolution nodes and colour options to support a portfolio of products.

The PYTHON family has more than 40 options, with resolutions ranging from VGA to more than 25Mpixel. These devices are available in multiple configurations, including monochrome, Bayer Color and extended NIR sensitivities. Selected devices are available in low-power configurations or with removable tape to protect the image sensor during the camera assembly process.

To help designers understand the performance available from the PYTHON family of image sensors, Avnet Silica offers a range of evaluation kits. These kits include an image sensor, the appropriate sensor headboard, FPGA evaluation board and software and accessories. The flexible design also allows the evaluation hardware to be use with other PYTHON devices by purchasing additional image sensors.

After identifying the most appropriate image sensor, designers then need to consider the remainder of the camera design. Complementary products from ON Semiconductor include embedded boards, power and signal chain components that allow engineers to choose between modular solutions and the flexibility of a discrete design.

If a machine vision system needs to be brought to market quickly, it may not be possible to build it from the ground up. For those applications, Avnet Silica products such as the PYTHON-1300-C camera module. Based on the PYTHON 1300 colour image sensor and featuring a 0.5in SXGA CMOS image sensor with a resolution of 1280 x 1024 pixels, the module can be combined with Avnet Silica’s MicroZed Embedded Vision Carrier Card and the Smart Vision Development Kit to provide a complete hardware design, leaving the designer to only write the application software.

While CCD image sensors may still remain preferable in some specialised applications, the combination of image quality, bandwidth, imaging flexibility and configuration flexibility available from CMOS image sensors has accelerated adoption of this technology in machine vision applications.

The imaging capabilities of such devices has ushered in a new level of performance and functionality for industrial imaging and CMOS sensor based imaging is now suitable for use in almost every type of design.

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Oxford University Innovation continues to impress with a growing list of spin out formations. Why is Oxford so successful?
By Neil Tyler.

Oxford University has a reputation not only as an internationally recognised seat of learning but increasingly as a hotbed of commercial innovation and small business creation.

Academics and researchers looking to commercialise their IP are able to turn to Oxford University Innovation (OUI) to get support. IP commercialisation is supported by its Licensing and Ventures team that can advise and help not only on licensing but on spinout formation as well, and crucially, OUI provides a point of contact where technologists and investors can meet.

It’s working with investors who are interested in early-stage ventures where OUI has been particularly successful. A specialised team helps new businesses to interact with the Angels Network, while the University’s own investment fund provides a valuable source of finance. An OUI Incubator not only supports ideas from within the university, but also provides support for traditional start-ups from the wider community.

OUI created 21 spinouts in 2016, up from five in 2016 and eight in 2014, and was involved in more than 855 deals which covered technology licenses and consulting deals and managed 2873 patents and patent applications.

Licensing plays an important role, but if the technology is strong enough to support a new company, then OUI will encourage the spinout option.

Since it was founded in 2007, OUI has created nearly 150 spinouts which have gone on to raise £1.5billion in external funding. Those companies have an estimated global turnover in excess of £600million.

The companies benefitting from the support from OUI are varied and include the likes of Bodle Technologies and Metaboards.

Bodle Technologies has developed a display technology that significantly reduces the power needed by a smartphone screen by using electrical pulses that need next to no power.

“We were spun out of the University back in 2015,” explains Richard Holliday, VP Business Development and IP, “and OUI was instrumental in the development of the business. After initial seed funding, we’ve embarked on a number of key funding rounds and the University has been integral in our success.

“We were spun out of the University back in 2015,” explains Richard Holliday, VP Business Development and IP, “and OUI was instrumental in the development of the business. After initial seed funding, we’ve embarked on a number of key funding rounds and the University has been integral in our success.

“OUI is there to guide academics looking to take an idea or concept to the wider world. Spinouts are formed out of the passion and IP of inventors and OUI is there to guide them. It has years of experience when it comes to knowing how to do things right and how, potentially, things can go wrong.

“Its role is to guide the investment process and, crucially, to protect the IP. It provides a network of investors and, as such, really pulls everything together.”

OUI will assign a project manager to a promising technology and then take it from development to incorporation. At the point where a company is set up, it will take a step back. But then how do you value a spinout? It’s certainly an interesting debate, agrees Holliday.

“How you value the worth of an invention and the business will depend on which applications you are going after. Ours is a platform technology and could be applied to electronic displays, security and smart glazing. Where the priorities are for a specific application is an important debate and OUI has a role in providing focus and building plans.

“Spinouts need a clear sense of direction,” says Holliday.
Once a patent is filed, there can be a long gestation period before a company is formed to exploit it commercially.

“Timing is another important issue,” Holliday concedes. “Bodle benefitted from an article in Nature, a high impact publication. That media coverage stimulated interest from potential end users and was influential in starting up the business sooner, rather than later.”

While market pull is crucial for some spinouts, it’s not always the case. “Look at quantum technology. While a lot is happening in that space and there are plenty of spinouts working there, practical applications of that technology are a long way away.”

**Metamaterials**

Tristan Collins is CEO of Metaboards, another spinout from Oxford University which is developing a wireless energy transfer technology using metamaterials.

“Metaboards was formed to commercialise IP from work conducted at the University,” explains Collins. “Our focus is on wireless power and data and using different surfaces as a conduit. We are looking to create an enabling technology behind a system of ubiquitous power and data. Currently, we are at the stage of looking to develop first products.”

The company uses metamaterials, or engineered materials, which is a relatively new area of science to develop its products.

The company’s founders include pioneers in the science of metamaterials and are experts in magnet inductive waves.

“One of our founders has been working in this field for 50 years, but it is only today that the technology is manufacturable,” Collins explains.

Officially spun out at the end of 2016, Metaboards has received seed funding from OUI and Collins was asked by the university to assess the viability of the technology.

“OUI had been looking around for interesting technology and asked me to look at the work being carried out, to identify interesting commercial opportunities and whether there was a route to commercialisation. Wireless power was the obvious one and the capabilities available to the business lent themselves to this.

“Through OUI, we got funding and access to investors to whom we could pitch our ideas.

“Over the past year, that support has enabled us to spinout from the university, support knowledge transfer from the academics into the company allowing us to then go off and commercialise that technology, start recruiting and continue academic work developing new patents,” Collins says.

“OUI also has board representation from a licensing point of view and help with managing the patent portfolio. We work together to ensure our interests are met and we get guidance and introductions through the university’s network.”

According to Holliday and Collins, while more spinouts are appearing, it’s still challenging and both accept that Oxford has provided their companies with a unique environment.

“There are certainly more spinouts appearing; some are IP rich, others less so,” suggests Collins. “Coming out of Oxford, I think we are sheltered from certain issues that the wider community would have to contend with. The downside to that is that we don’t get the media coverage that the Silicon Roundabout hub in London gets.

“Despite that, it would have been a lot harder for us without Oxford. Without a doubt, OUI is well connected, it can make things happen and it works on a global stage.”

Outside the university eco system, just one in three businesses succeeds.

“Oxford provides all the key ingredients to be successful. From academic excellence and an impressive science base to a growing international investor base – funds from around the world are looking to invest in Oxford technology,” says Holliday. “I think Oxford reflects a wider societal change and more academics are interested in starting their own businesses.

“But while the monetary awards are attractive, for many academics it’s about seeing their breakthroughs make it into the wider world.”

“It’s also true to say that a lot of inventions get patented but don’t end up in a company, some will be licensed to SMEs or large corporates,” says Collins. “But for many that is a preferable way of getting their technology to market.”

“We’re learning from the US experience,” Collins believes, “and spinouts are helped by the fact that universities are now more business savvy. They realise that by backing spinouts not only do they provide a source of revenue, but they are also helping academics get their ideas into the wider world and to provide career development for research students. It’s a win-win scenario.”
When he was a student in the mid-1990s, Paul Kocher tried to support his veterinary studies at Stanford University with consultancy work in what was then a side interest of cryptography. As the dot-com boom took hold, so too did the work of discovering flaws in clients’ security mechanisms.

A presentation at the university on using differences in inputs to try to detect the changes made by encryption algorithms led him to try out new types of attack. While his PC was not up to the task, he realised that bigger differences might be found in how long encryption algorithms took to do each job.

Kocher put into action an idea that first emerged more than 40 years earlier. In 1949, US Armed Forces Security Agency staffer Ryon Page noticed the changes in sound made by rotor-based cipher machines as they worked and thought it might be possible to recover plain text from the noises alone. Sound, however, did not emerge as an attack vector until 2013, when cryptographer Adi Shamir developed an attack based on the subtle warbling of a power supply transformer.

Kocher focused on differences in timing; by comparing the time it took to complete each of a thousand or so encryptions, an attacker could discover the supposedly private key they used.

Today, the variety and scope of attacks has exploded and all manner of eavesdropping channels – known generically as side channels – are now in use. Power, electromagnetic emission and even sound can reveal enough about the internal operation of a system to break encryption keys, although these often rely on more sophisticated analysis of tiny changes in performance over time to try to glean information among the inevitable surrounding noise.

Timing remains the most pervasive form of attack, largely because of the rise of the internet. Early attacks relied on physical access to devices that were, for the most part, never going to be connected to a two-way network. One example lay in pay-TV, where breaking the keys could lead to millions in sales of counterfeit cards. The rise of the smartcard led to other financial targets, which then needed to build in stronger defences.

“There is no market where people take security more seriously than payment,” says Don Loomis, vice president of micros, security and software at Maxim Integrated.

The internet, however, provided a link between side-channel attacks and remote-controlled spyware. And it supplies a much richer variety of potential victims in industries where the attention to attacks based on side channels is far more limited. In these attacks, time is not necessarily the leakiest side channel, but it is the easiest to access.

In a typical cloud-based attack, some form of spyware is uploaded to a cloud server that monitors how other applications running on the same blade use caches and memory. An attack such as Prime+Probe, developed a decade ago by Dag Arne Osvik and colleagues from the Weizmann Institute of Science in Israel, has the spyware fill a cache bank with its own data and then watches how the activity of the victim program displaces different cache lines.

Although spyware will usually be prevented from reading cache lines it does not own, it can probe which lines have been altered by a different task by timing how long it takes to access data from its own memory pool. If a read takes a long time because data needs to be pulled back from main memory, it demonstrates the other process evicted its data in order to change one of the targeted variables.
Changes in access patterns outline the spyware the internal decisions the victim program is making and so let it trace execution without having to see the data the victim is running.

Now side-channel attacks have shifted to the smartphone. Veelasha Moonsamy, a researcher at Radboud University, says devices like smartphones have properties that make them vulnerable not just to the kinds of locals attacks that plague smartcards and traditional embedded systems but those used to exploit cloud applications (see fig 1). And there is a much richer pool of leaky channels in the shape of the many motion and environmental sensors they now contain. Spyware on the device that can gain access to the same sensor readings as the foreground app can use them to work out how the user is interacting with the device and pick up supposedly secure information.

Figure 1: Smartphones have properties that make them vulnerable to attacks used to exploit cloud applications

![Diagram](image_url)

Even when the device is meant to be inactive, a public USB-based charging station provides one of a number of ways to gain physical access and probe it. Researchers at the College of William and Mary and the New York Institute of Technology published a proof-of-concept attack a year ago that used power fluctuations on the USB charging cable — even with hardware protection to prevent actual data transfer — to work out which web pages the user was visiting. Another attack developed by Moonsamy and colleagues for locker-type public chargers used a trojan app on the phone that could signal covertly to the charging station while it probed background tasks.

The key to fighting side-channel attacks lies in restricting the amount of information an attacker can pick up from measuring differences. Removing sources of difference is the most effective way to do this. This is often done by removing branches that indicate different decisions being taken or performing dummy activities to disguise the use of less power-hungry operations. However, this is not entirely secure.

Circuitry that is prone to glitches can leak power information to a local attacker, as can changes in data from cycle to cycle. A large Hamming distance between successive values passed along a bus will consume more power than a transfer of words that share all but a few common bits. Hardened circuit designs focus on such low-level attributes with glitch-free logic and encrypted buses.

Recognising the likelihood that the next jump in terms of attacks will be to devices intended for the IoT, Maxim has built countermeasures into its low-end DeepCover chip, designed to protect against counterfeiting. But most off-the-shelf microcontrollers are not designed with side-channel protection in mind, although firmware writers can take simple measures to hinder attackers.

Hugo Fiennes, CEO of secure-hardware platform provider Electric Imp, says: “Many customers don’t want to pay for the hardened hardware. But a lot of side-channel attacks rely on being able to run back-to-back crypto operations rapidly. We deal with that by making that hard to do on the platform. It helps a little.”

Another approach is to detect behaviour that indicates an attack is being deployed, such as unusual cache-access patterns or software continually running the encryption unit to try to create enough traces for analysis. A protected device may reset or wipe its keys to terminate the attack. However, these can undermine reliable behaviour by triggering on false positives.

A research project at the University of Bristol aims to bring make it easier to bring software-level countermeasures to IoT and embedded devices, even if hardware hardening does not justify the cost. David McCann and colleagues added power estimation into a version of the open-source Thumbulator, based on data collected from execution traces of the ARM Cortex M0 and M4.

Explaining the motivation at last summer’s Usenix Security conference, team member Carolyn Whitnall said: “What we’ve been aiming for is to equip software designers with the ability to detect side-channel vulnerabilities in the development stage and provide an opportunity to make security enhancing adjustments while it is still relatively cheap and easy to do.”

The problem for IoT and embedded systems designers is that it’s relatively cheap and easy to mount attacks.

Vigilance and more careful design will push the cost up for the hacker and limit their rewards.
Ensuring software quality

As the software component in new products explodes, how can companies ensure code quality when they are faced by time-to-market challenges? By Neil Tyler.

Over the past 30 years, the use of tools that help engineers to simplify and automate the design, development and integration process has propelled the development and manufacture of electronics and embedded systems. Today, when the concept of quality is becoming critical to all aspects of business, we are seeing the same developments when it comes to ensuring quality software development.

“Across all industries, software content is exploding and it’s not just the amount, but also the criticality of the software being deployed,” explains Jeff Fortin, head of product management at Vector Software. “More companies are looking to use software to differentiate the value being provided in embedded devices.”

The importance of software in delivering key features and systems, including safety critical functions across many different pieces of equipment and systems, means the traditional ‘artisan’ approach to software development is being abandoned.

In that approach, software development was viewed as more of a creative process. Today, software needs to be constructed with the precision and quality typically associated with modern-day manufacturing.

Regular news reports of product recalls due to software bugs, show that issues around testing remain. When investigated, many of these recalls can be attributed to issues that should have been picked up in quality testing but ‘time-to-market’ pressures meant the software didn’t receive sufficient testing before being deployed.

“Customers are under pressure to develop products faster to meet the needs of new business models,” according to Fortin. “Succumbing to market pressure to develop software quickly is full of risks. Poor quality software leads to failures and expensive product recalls, as well as reputational damage.”

Embedded systems commentator Jack Ganssie notes: “Eighty percent of embedded systems are delivered late and new code has 50 to 100 bugs per thousand lines.”

“We’ve seen examples of test code being left in place and then being deployed in the real system – suggesting a lack of time to test the...
That raises the question of how do you address the needs of new business models while maintaining quality using existing tests?

“Do they need to run all the safety tests if they are looking to upgrade software in the field? How do we do the testing efficiently, whilst not impacting on the quality of that testing?” Fortin asks.

Maintaining quality

Engineers and developers need tools that afford them the visibility of testing completeness as well as the generation of test cases for code that are not covered by existing test cases.

But, as experience shows, tests do not guarantee bug-free code at the end of the day.

“The majority of problems with an end product are usually caused by inefficient and incomplete software testing,” suggests Fortin. “It’s the efficiency or agility of this part of the development process which defines how quickly products are developed, assembled and then released – and it’s this part of the process that is under the greatest pressure to deliver.”

Without proper testing, quality issues will not be detected, which means that reworking and retesting will result in a slowing down of the speed of delivery.

“We are seeing more companies trying to achieve a six-week release cycle when, realistically, it will take three months to carry out every test that is required,” says Fortin.

Engineers need to be able to run tests on a simulation to verify the system’s behaviour and compliance with the requirements set out.

Furthermore, as products develop over their lifecycle with upgrades or availability of new features, changes will need to be made and implemented. These changes have code implications and engineers will need to understand where source code changes will have knock-on effects and be able to create new tests to test the new code.

A designated software testing platform allows engineers to overlay intelligence that understands the smallest number of tests to be re-run by a change to the source code.

So, what can development teams do to ensure they have the agility, process and tools that allow them to ensure development tasks can be done in the fastest time and to the highest quality standards?

Various toolsets are available and they provide designers with a comprehensive range of automated software testing tools that enable the implementation of a complete and automated test infrastructure.

“VectorCAST, for example, provides users with the ability to check the health of their codes by using heat maps, dynamic dashboards along with in-depth analytics that provide actionable data for improving code quality,” explains Fortin.

“VectorCAST2018, our first major release since 2015, looks to consolidate many new features in a fully integrated package that offers embedded software development teams the functionality to create their own bespoke systems test and QA environment,” says Fortin.

“This new integrated environment can run whatever tests are required to ensure software meets the requirements specified, satisfies market demand and, in doing so, protects the brand’s reputation.”

Ease of use has been an issue, so this latest update has sought to simplify the user interface and looks at enabling more people to access the testing process.

“More people running tests means a greater chance of finding problems,” Fortin argues. “We wanted to make the testing process as easy to use as possible. Testing is complicated and we wanted to make the tools a little ‘softer’ for people to use, as well as using automation more efficiently.

“We didn’t want to isolate the testing function to a few people, so with a simple click, all system level and unit level testing is available to users.”

A key component of VectorCAST 2018 is support for greater parallelisation in terms of both systems and unit level tests.

“We wanted to be able to run these tests efficiently and be able to test pieces of the code in parallel,” says Fortin.

Fortin believes that tools like VectorCAST will, in time, provide more of the background calculations testing, while providing continuous testing and integration. While these improvements should make the testing environment easier, users will still have to contend with a regulatory environment.

“We have to accept that regulators don’t move at the pace which the market demands, creating a stress between where the market wants to go and where regulations stand. But what we can do is make the work undertaken by engineers as efficient as possible.

“Looking to the future, a vast amount of test generation and reporting will be automated, the trickier part will be ensuring that the tests being run are the correct ones.”

Jeff Fortin
As optical networks, hyperscale data centres and mobile fronthaul/backhaul networks move to higher data rates to support rapidly increasing Internet traffic demands, SerDes reference clock performance is becoming increasingly important.

If reference clock jitter is too high, it results in unacceptably high system bit-error rate (BER), lost traffic or loss of system communication.

In addition, 56G PAM4 PHYs, 100G/200G/400G Ethernet, and 100G/400G OTN require a more diverse mix of frequencies, increasing timing complexity.

The Si54x Ultra Series of oscillator products from Silicon Labs is purpose-built to address the needs of these demanding high-speed communications and data centre applications.

These high-performance oscillators offer any-frequency synthesis, ultra-low jitter of 80fs rms and are available in standard, small form factor oscillator footprints. By providing best-in-class jitter margin and frequency flexibility, the Ultra series is intended to make it easy for hardware designers to de-risk product development.

The device can be programmed and customised to meet the target frequency during outgoing test and, by using this approach, the Si54x can be mass customised in order to meet each customer’s requirements.

The Si54x Ultra series supports any frequency from 200kHz to 1.5GHz, enabling a single product family to support both standard and custom frequency applications.

Designed in 55nm CMOS technology, the fourth generation DSPLL leverages a highly digital architecture to deliver improved frequency flexibility and jitter performance.

The input to the DSPLL’s phase detector is converted from analogue to digital, enabling the DSPLL to operate entirely in the digital domain and this all-digital approach has multiple benefits for the design engineer.

First, the digitally controlled

### High-speed communications and data centre timing requirements

<table>
<thead>
<tr>
<th>Standard</th>
<th>Data Rate</th>
<th>Target frequencies</th>
<th>Reference clock max phase jitter*</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEI-28G</td>
<td>28Gbit/s</td>
<td>106.25MHz</td>
<td>150fs</td>
</tr>
<tr>
<td>CEI-56G PAM4</td>
<td>56Gbit/s</td>
<td>125.00MHz</td>
<td>150fs</td>
</tr>
<tr>
<td>100G Ethernet</td>
<td>4x25.8Gbit/s</td>
<td>156.25MHz</td>
<td>180fs</td>
</tr>
<tr>
<td>CAUI-4</td>
<td>4x25.8Gbit/s</td>
<td>161.1328MHz</td>
<td>240fs</td>
</tr>
<tr>
<td>16G Fibre Channel</td>
<td>14.0Gbit/s</td>
<td>175MHz</td>
<td>240fs</td>
</tr>
<tr>
<td>32G Fibre Channel</td>
<td>25.6Gbit/s</td>
<td>200MHz</td>
<td>130fs</td>
</tr>
<tr>
<td>Infiniband EDR</td>
<td>25.8Gbit/s</td>
<td>322.265625MHz</td>
<td>180fs</td>
</tr>
<tr>
<td>Rapid IO-4</td>
<td>25.3125Gbit/s</td>
<td>644.53125MHz</td>
<td>290fs</td>
</tr>
<tr>
<td>SONET OC-192</td>
<td>9.953Gbit/s</td>
<td></td>
<td>240fs</td>
</tr>
</tbody>
</table>

*Note: Calculated directly from reference clock or transmitter eye closure specifications budgeting eye closure 50/50 deterministic/rms and 33%/67% clock/transmitter per raw (pre-FEC) BER requirements.

### Author profile:
James Wilson is marketing director, timing products, with Silicon Labs.
oscillator (DCO) can be precisely steered with a step size as small as 1ppb to track out phase delay between the reference and feedback clocks. The DCO gain is small, making the circuit less susceptible to noise than conventional analogue PLLs.

Secondly, the DSPLL supports an innovative phase error cancellation circuit that uses advanced digital signal processing to remove PLL noise due to delay, non-linearity, and temperature effects.

These architectural features ensure consistent device performance across process, voltage and temperature and, as a result, Silicon Labs’ fourth generation DSPLL architecture delivers ultra low jitter across the entire operating range.

When it comes to jitter performance versus operating frequency and temperature, the Ultra series comes with two performance grades. Si545/6/7 devices provide a typical phase jitter performance of 80fs rms (12kHz to 20MHz), whereas Si540/1/2 devices provide a typical jitter performance of 125fs rms (12kHz to 20MHz). Given their jitter performance, the Si54x has been designed to maximise jitter margin.

Below: The Ultra series DSPLL architecture

To further simplify device evaluation, Silicon Labs also offers an XO phase noise lookup utility that can be used to retrieve more than 1000 measured phase noise plots of oscillators across a wide range of popular frequencies.

Integrated power supply noise regulation
The DSPLL also comes with an extensive network of on-chip low drop out regulators to provide power supply noise rejection, ensuring consistently low jitter operation even in noisy system environments.

Another benefit of integrated power supply noise regulation is simplified power supply filtering, PCB design and layout.

Multi-frequency support
In addition to standard single frequency oscillators, dual and quad frequency oscillators leveraging Silicon Labs’ DSPLL architecture are available. These devices can replace two or more discrete oscillators with a single IC, helping to minimise both BOM cost and complexity.

Multiple benefits are offered by multi-frequency oscillators, including:

- Support multi-protocol SerDes with single device
- Simplified set up/hold time testing
- Frequency margining (for example, 156.25MHz ±50 ppm, 156.25MHz, 156.25MHz -50 ppm)
- Simplified prototyping. Testing new SerDes and ASICs with a variety of reference clocks using a multi frequency oscillator. Transition to a fixed, single frequency oscillator once the final frequency is selected.

Wide range of format options
Silicon Labs’ Ultra Series oscillators have a flexible output driver that can be factory customised to support any common signalling format, including LVDS, LVPECL, HCSL, CML, CMOS and dual CMOS.

In addition, the output driver supports a wide supply voltage range. A single Si54x device can support 1.8V to 3.3V operation, enabling a single part number to replace multiple fixed voltage 1.8V, 2.5V and 3.3V oscillators.

As the demand for oscillators grows so manufacturers are looking to offer a one-stop shop for high performance oscillators to meet the needs of design engineers.
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