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In the ‘Year of Engineering’, engineering skills are taking centre stage and the Skills Commission inquiry, which is co-chaired by Lucy Allan MP, Preet Gill MP and Professor Sandra McNally, is taking evidence as to why women are so badly under-represented within engineering courses, and whether upcoming skills system reforms will encourage more women to go into the profession.

Last month, the Provost of NMiTE, the new engineering university being created in Hereford, gave evidence to the commission and, according to Professor Elena Rodriguez-Falcon, the imbalance between the number of male and female engineers is due to a misconception among teenagers as to what constitutes a professional engineer. As a result, many were rejecting engineering as a career.

She dismissed what she called the dogmatic insistence in the UK that, “all engineers must have A-Level Physics and Maths.”

While professional and competent engineers need to know when to use maths and what maths to use, she wondered whether A-Levels were the only way of ensuring this.

“Too few female teenagers are inspired to take Maths and Physics A-Level, partly because they don’t see it leading to the sorts of careers they want,” according to the Professor.

A new report, from the Institute of Physics (IoP) ‘Why Not Physics? - A Snapshot of Girls’ Uptake at A-level’, has found that only 1.9% of girls chose A-Level Physics in 2016, compared with 6.5% of boys.

Even more shocking was that 44% of schools in England send no girls at all to study the subject.

So how do we close the gender gap when Britain has an estimated shortfall of 40,000 engineering graduates?

Without serious and sustained intervention, the gender gap is likely to persist for generations. A lack of visibility also preserves the myth that Physics is “not a subject for girls.”

NMiTE plans a radical approach based on the success of the Olin engineering college in America, which consistently achieves a balanced intake of male and female students.

NMiTE is looking to attract a much broader intake of people, rather than only drawing from the limited pool of sixth-formers doing A-Level Maths in what is a very specialised syllabus.

Its approach can be summed up as “100% learning by doing: no lectures, no set textbooks, and no exams,” and creating a syllabus based on the real world needs of industry.

Olin has been cited as a role model, and while it is a relatively new college, it’s around 20 years old it has a growing reputation for engineering and the admission process is very competitive. In fact, a report from MIT said that Olin College was now among the leading institutions for teaching of engineering in the US.

Radical change is needed because the lack of girls studying Physics to a higher level will have real consequences for the UK economy, but not only that, the consequences of girls’ choices at school mean that many are missing out on a rewarding and fulfilling career.

Neil Tyler, Editor (neil.tyler@markallengroup.com)
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AI Accelerator for Edge computing

SOCIONEXT DEVELOPS AN AI ACCELERATOR ENGINE FOR EDGE COMPUTING.

NEIL TYLER REPORTS

Socionext has developed a new Neural Network Accelerator (NNA) engine, that has been optimised for AI processing on Edge computing devices.

The engine is both compact and low power and has been designed specifically for deep learning inference processing. When implemented, it can achieve 100x performance boost compared with conventional processors for computer vision processing such as image recognition.

Socionext currently provides graphics SoC “SC1810” with a built-in proprietary Vision Processor Unit (VPU) compatible with the computer vision API “OpenVX” developed by the Khronos Group, a standardisation organisation.

The NNA has been designed to work as an accelerator to extend the capability of the VPU. It performs various computer vision processing functions with deep learning, as well as conventional image recognition, for applications including automotive and digital signage, delivering higher performance and lower power consumption.

The NNA incorporates the company’s proprietary architecture using its quantization technology to reduce the bits for parameters and activations required for deep learning.

The quantization technology can carry out massive amounts of computing tasks with less resource, greatly reducing the data size, and significantly lowering the system memory bandwidth.

Socionext is planning to start delivering a Software Development Kit for the NNA FPGA implementation in the third quarter of 2018 and is looking to deliver SoC products which incorporate the NNA.

Chip resistor warning

Anglia Components is advising its customers that they should be looking to ensure that they have sufficient orders/inventory to cover their chip resistor needs.

Global demand for resistors is currently massively outstripping supply. Shortages and price increases are already heavily impacting various applications. Material prices are also on the rise, driven by the increase in demand, creating a situation whereby chip resistors will remain in short supply and prices will continue increasing in the short to medium term.

Pinch of salt

Salt can be used to improve the performance of batteries, claim researchers from the Queen Mary University of London, University of Cambridge, and Max Planck Institute for Solid State Research.

By adding salt to the inside of a supermolecular sponge and then baking it at a high temperature, the sponge transformed into a carbon-based structure.

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Batteries not only enable the batteries to be charged-up rapidly, but also at one of the highest capacities.

Due to their intricate architecture, the structures have been termed ‘nano-diatoms’, and believe they could be used in energy storage and conversion, for example as electrocatalysts for hydrogen production.

The sponge used in the study is also known as a metal organic framework (MOF) material. By adding salts to these MOF sponges and carbonising them, the researchers say they discovered a series of carbon-based materials with multiple levels of hierarchy.
ON Semi has acquired SensL

ON Semiconductor has acquired SensL Technologies. SensL, based in Ireland, is a technology company specialising in Silicon Photomultipliers (SiPM), Single Photon Avalanche Diode (SPAD) and LiDAR sensing products for automotive, medical, industrial and consumer markets.

The acquisition will help to extend ON Semi’s position in the market for automotive sensing applications for ADAS and autonomous driving with expanded capabilities in imaging, radar and LiDAR.

OnSemi has previously acquired radar technology and design centres in both Israel and the United Kingdom.

Battery-free smart toys

Specialised nanogenerators that gather energy from mechanical vibrations have been used to transform conventional children’s toys into ‘smart’ electronics. A report in ACS Sustainable Chemistry & Engineering said the findings could have broad commercial applications, leading to the development of battery-free, self-powered toys, medical sensors and other devices.

The researchers designed and incorporated triboelectric nanogenerators or TENGs – which gather electrical charges from friction and amplify and convert this biomechanical energy into a usable form – into toys.

The TENGs were made with aluminium electrodes and an eco-friendly silicone-like film was placed between them. Squeezing or shaking the toys alternately separated and brought the electrodes into contact with the film, creating an electrical charge.

Once activated, the TENGs harvested enough biomechanical energy to illuminate several LED lights attached to each toy. The TENGs were durable, suggesting they could operate for an extended period of time.

Lattice on the Edge

THE INDUSTRY IS CALLING FOR A NEW KIND OF AI SOLUTION FOR THE EDGE AND LATTICE SEMICONDUCTOR AIMS TO DELIVER.

BETHAN GRYLLS REPORTS

The demand for Edge computing is being driven by the need for improved latency, privacy and bandwidth options, said Deepak Boppana, Senior Director, Product and Segment Marketing of Lattice Semiconductor.

In response, Lattice has released the sensAI – a complete technology stack that combines modular hardware kits, neural network IP cores, software tools, reference designs, and custom design services – that is based on its existing low power FPGAs.

“We have long-term expertise in Edge connectivity,” Boppana said. “We are already providing sensor bridging and aggregation, now we are integrating intelligence into the FPGAs. Designers want technology that seamlessly fits into their existing architecture, they don’t want to turn their designs upside down just for the sake of adding AI.”

sensAI is designed to fit in with the applications requirements, with power consumption ranging from 1mW to 1W, package sizes from 5.5mm² to 100mm², interface flexibility (MIPI CSI-2, LVDS, GigaE, etc.), and high-volume pricing ($1 to $10).

The stack will be downloadable from the Lattice website. “We want to make AI accessible for everyone,” Boppana said. “sensAI is for applications that care about cost and ultra-low power, but also want a programmable, flexible platform.”

The idea is that the sensAI will accelerate the integration of machine learning inferencing into the broader market for Internet of Things applications.

Transforming farming

Small Robot Company, a British ‘agri-tech’ start-up for sustainable farming, has launched an Indiegogo campaign to fund its digital planting robot ‘Harry’.

The Small Robot Company is seeking £50,000 backing on Indiegogo to commercialise Harry, which it says will accurately place seed individually in the ground at a uniform depth to within 2cm accuracy, creating a plant level map showing the location of each seed. By punch-planting rather than ploughing, Harry should also reduce soil run off and associated water pollution.

“We want to revolutionise the way that technology is used to create food, reducing the cost to the environment,” says Co-Founder, Ben Scott-Robinson. “Current arable farming methods, in particular ploughing and blanket spraying, are extremely harmful to the environment.”

Small Robot Company’s robots work alongside an artificial intelligent ‘nervous system’, Wilma, to ‘digitise the field’ and provide a granular digital view of the farm. The technology employs a range of farming knowledge, including agronomy, soil science and market conditions, coupled with aggregated big data from all farms across the country, and applies it to the information gathered about the crop.

“Our vision is to automate and digitise arable crop farming,” says co-founder Sam Watson Jones. “Farming is arguably the last analogue industry. The potential for efficiency here is phenomenal, and the environmental benefits this then bestows are immense. Simply put, it’s the ability to apply permaculture techniques at scale. It’s the ultimate sustainable farming model.”
PCBDM Live strikes the right note

INAUGURAL PCB DESIGN AND MANUFACTURING LIVE SHOW GETS THE THUMBS UP FROM VISITORS AND EXHIBITORS ALIKE. BETHAN GRYLLS REPORTS

PCB Design and Manufacturing (PCBDM) Live, organised by New Electronics and held at the National Motorcycle Museum in Birmingham earlier this month, proved popular with visitors and exhibitors alike.

Running alongside the show was a programme of seminars which included speakers: Tony Folan from Altium; Gary Hinde from Cadence; Hugh Macdonald and David Strachan from Plexus; and Tom Gregory of Future Facilities.

Focusing on PCB design Gregory outlined the importance of checking for modelling errors in a system before proceeding with the design. Hinde showed designers how to easily identify and fix impedance mismatches, crosstalk and return path issues using approaches that provide impedance vision, coupling vision and return path DRCs.

A broad range of PCB suppliers were in attendance and used the show to exhibit some of their latest kit. Those at the show included: Beta LAYOUT; Toby Electronics and Nexus, among others.

Phoenix Contact demonstrated its twin design print terminals, which offer either a screw-in or a push-in that has the same footprint on the PCB, meaning suitable connection technology can be chosen without changing the board.

Hitaltech exhibited its flexible interconnect products, intended for panel design formats. The boards can be “broken” and folded, before being placed into an enclosure, acting as a flexible alternative to a rigid board-to-board header and socket.

With upwards of 800 visitors, PCBDM Live is set to return next year.

Semiconductor ribbons

Scientists from the National University of Singapore (NUS) have discovered a unique growth mechanism to produce atomically thin semiconductor ribbons that can serve as a building block for high-performance nanoelectronic devices.

According to NUS, growing nano- and micro-ribbon structures of molybdenum disulphide, involves the reaction of sulphur vapour with a mixture of molybdenum trioxide and sodium chloride salt at ~700°C on a clean crystal surface.

The morphology of the narrow ribbons was unlike what is normally expected from a vapour-liquid-solid growth, and indicates that the liquid droplet moves on the substrate surface in an ordered manner.

The researchers demonstrated that high-performance microscopic transistors (with a field effect mobility of ~30 cm²/Vs and on-off ratio of ~10^6) can be fabricated from the individual ribbons. Because the as-synthesised material is already in the shape suitable for the device, fabrication is possible without the need for an extra patterning step.
Box-shaped robots sliding like rooks on a chessboard made of crates, pulling the boxes up with “fingers” from the stack and into a cavity within them, before delivering them to pick stations. Welcome to Ocado Technology’s Andover facility.

The “swarm” of round 440 robots, live in a 2D world, Paul Clarke, Chief Technology Officer (CTO) explains; moving on a horizontal or vertical axis, collecting, delivering and replenishing storage on a SIL 3 safety certified grid or “hive”.

The robots can accelerate up to 2m/s² reaching speeds of 4m/s, with millimetre tolerances. But it was making a grid the size of a football pitch, while still ensuring the robots could pass each other at a 5mm distance and within 60cm of the roof beams, that was the biggest challenge, according to Clarke.

Each bot is exactly the same, so are easily replaced by another if, for example, maintenance, charging or updates are required. The robots can also collaborate in swarm-like behaviour to carry out tasks which require more than one bot to complete.

In terms of the software stack, the low-level software that controls the robot is written in C, while the high level overall control software is written in Java. OpenStack is used to provision an internal cloud infrastructure where Ocado uses Kubernetes to create containers for the applications it needs to run. Log data is stored in Ceph and everything is streamed into Google Cloud where Ocado uses BigQuery for analytics.

The communications network is said to be the world’s first deployment of unlicensed 4G spectrum for warehouse automation. The wireless protocol uses orthogonal frequency-division multiple access (OFDMA) which is used by LTE for the downlink air-interface. However, Ocado has replaced the media access control (MAC) layer with its own implementation and entirely removed the upper layers of the 4G cellular offering, which were not relevant for this particular project.

The system has the notion of a resource map where the frequency and time allocation for each node is described. Ocado’s wireless protocol’s map is fixed for each client as it adds it to the system vs LTE or WiMAX where some element of scheduling is involved.

Before physically building this high-tech warehouse, Ocado’s simulation team created a 3D representation of the structure, which was used to develop and test software. The simulation was then transformed into a live monitoring system, meaning Ocado can track what every bot is doing in real-time and anticipate issues.

This technology is part of the Ocado Smart Platform (OSP), a solution designed to power the online grocery business of retailers around the world.

Previously, Ocado would purchase third party hardware from logistics companies and install them in the warehouses. A solution that worked well in both its Hatfield and Dordon factories, Clarke points out. But for the OSP, Clarke says it needed to control the supply chain and to design a solution that could easily be installed and scaled in any geography, as well as suitable for overseas operations.

“We use one machine to design, evolve, manufacture and support, making it a much more flexible and accessible solution” he explains. “We want to be able to sell this system into territories where online grocery is more nascent. With OSP, a company is able to build upon the hive in stages, partially populating it until the need to expand arises, when they can just add more robots and crates.”

Ocado has already licensed its OSP to several companies, including Morrisons, and intends to increase its own swarm to 1,100. The online grocery store believes at full capacity, it will be able to process 65,000 Ocado orders every week.

To talk to the robots, Ocado Technology designed what it claims is the “world’s densest mobile communications network based on 4G technology”. According to Ocado, the communications protocol guarantees a connection 10 times a second to each of the 1,000 robots per base station – all working within a 150-metre radius.
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Coal from South Wales drove the last industrial revolution, could the compound semiconductor cluster now being developed in the region, be set to deliver the next one? By Neil Tyler

Back in 1982 a semiconductor fabrication facility was built and opened near Newport in South Wales. The 8,900m² single storey building was originally a microprocessor facility for Inmos, but it soon changed hands passing from Thorn EMI then to STMicroelectronics, who used it to produce SRAM and other products.

International Rectifier then acquired the site in 2005 and used it as a R&D and manufacturing centre until Infineon bought the company, and the facility, in 2015.

The original development had promised thousands of new, highly skilled jobs and placements for apprentices, but over the years failed to deliver. Today, however, the site is home to Newport Wafer Fab and this facility is at the heart of what is being described by local politicians, academics and businessmen as the world’s first compound semiconductor cluster, or CS Connected.

CS Connected can be described as an umbrella organisation that represents organisations associated with research and development, and innovation and manufacturing of compound semiconductor related technologies, as well as those companies involved in the extended supply chain.

Almost a year since the decision to support this initiative was agreed, Dr Drew Nelson, CEO of IQE, an established leader in the development and manufacture of advanced semiconductor wafer products, believes that the efforts of business, policy makers, and academics are bearing fruit and helping to turn this and development ecosystem. CS Connected is about bringing them closer together.”

Those who see compound semiconductors as crucial in enabling and supporting future generation technologies, believe that this emerging cluster could place the region at the forefront of the next industrial revolution.

As a consequence, CS Connected, which has been driven in part by IQE and Cardiff University, has not only the backing of both the Welsh Government and the UK Government through Innovate UK, but also includes a growing number of businesses such as SPTS and Microsemi.

Other key bodies in the development of the hub include the Institute for Compound Semiconductors, the ESPRC Compound Semiconductor Hub, the Compound Semiconductor Centre (CSC) and the Compound Semiconductor Applications Catapult (CSA Catapult).

The region is aiming to become Europe’s first major cluster for firms developing compound semiconductors and is looking to attract private investment of almost £400 million, in turn creating 2000 skilled jobs in the process.
At the end of last year, IQE and the Welsh and UK governments, ratified the development of the Compound Semiconductor Foundry which will provide crucial support in the development of the CS Connected cluster.

So just what are compound semiconductors? Well, they are crucial to many of the devices that we take for granted today but which have a profound impact on the way in which people live.

Whether in smartphones or in satellites, compound semiconductors are set to play an increasingly important role, especially in the kind of technologies which are predicted to dominate the landscape in coming years, whether that’s robotics, electric vehicles, wearable technology, or the infrastructure to support 5G cellular networks.

Compound semiconductors will have a crucial part in this because not only can they process things faster than silicon, but they are more versatile and sensitive.

Working exactly like silicon chips, they are able to offer much higher levels of performance – being up to 100 times faster – hence their importance when it comes to high speed communications.

They also offer much better power efficiency and a wide range of optical properties for emitting and receiving light.

They can certainly be described as a revolutionising technology.

Atomically engineered materials are at the heart of compound semiconductors and can include a variety of elements such as gallium, indium, arsenic, phosphorus, nitrogen and silicon. By combining these elements it is possible to form compounds that are better able to meet the performance requirements of future technologies, which silicon, on its own, is unable to.

A growing market

“The market for compound semiconductors is worth an estimated £66 billion, and the UK has a market share of roughly around 9 per cent,” according to Dr Andy Selliars, Chief Business Development Officer at the CSA Catapult.

“With the demand for advanced power, photonics and RF devices set to accelerate, analysts expect the global market to reach $140bn by 2023. This will be further supported as the use of compound semiconductors expands into new markets.”

According to Alistair McGibbon, Business Development Manager, at the CSA Catapult, “We want to accelerate the introduction of compound semiconductor technology into advanced systems and ensure that the UK plays a central part in the developing global supply chain.

“Our role at the CSA Catapult is to provide a bridge between companies developing novel semiconductor materials, topologies and devices with those companies that are looking to develop applications and, where necessary, linking them with organisations looking to provide financial support.”

According to Dr Selliars, the UK has a: “Rich base of research on which to build applications. Around £750m has been invested over the past decade by ESPRC and Innovate UK in compound semiconductor technologies.”

The UK also has a good mix of SMEs and Tier One companies in this space. “We are currently engaging with many of them and I would expect to see that accelerate, going forward,” McGibbon suggests.

The Catapult, part of the UK’s nationwide network of technology innovation centres, and the first to be based in Wales, forms an essential pillar of the CS Connected cluster.

“The Catapult network was set up by Innovate UK to drive economic growth,” explains McGibbon, “and we are well positioned to exploit the UK’s recognised leadership in advanced electronics, science and innovation.”

The Catapult continues to receive a further boost when Infineon Technologies signed a definitive agreement with Neptune 6, the owners of the Newport Wafer Fab, under which the latter acquired the old International Rectifier (IR) site in Newport in the autumn of last year.

According to Sam Evans, Director of Quality & External Affairs, Newport Wafer Fab: “We want to be able to create a campus feel across the cluster, akin to that seen in the Fraunhofer in Germany, or imec in Leuven, Belgium. There, academia and industry come together and collaborate.

“There are plenty of skilled workers at the Newport and we have plenty of reliable and very experienced people to call on. That means it is well placed to contribute to the rapidly emerging cluster of companies in this part of Wales.

“The fab is well equipped and will be highly complementary to the existing semiconductor expertise
in the region. If we had to have developed a Greenfield facility here, then the costs associated with that would probably have been prohibitive.” Evans continues, “Newport Wafer Fab’s role in the cluster is to provide volume manufacturing services for companies that have created solutions using compound semiconductors.”

While South Wales is aiming to become a European cluster for firms developing compound semiconductors, there are currently four other recognised semiconductor clusters in Europe.

One is at Leuven in Belgium, another in Eindhoven in the Netherlands, and the others are in Dresden and Genoble.

“This, however, will be the first to specialise in compound semiconductors,” says Evans. “It is a world first.”

“Those regions in Europe are home to upwards of 800 high tech firms,” says Chris Meadows, Head of Open Innovation at IQE, “and together with academic institutions employ well over 150,000 highly skilled workers. They are a magnet for attracting both funding and future investment.

“What we are trying to achieve here in South Wales will be unique. It’s an opportunity, not only for Wales, but for the UK and Europe.

“We want to harness the existing expertise in compound semiconductor technology to create a major high tech compound semiconductor cluster and then develop a pan-European compound semiconductor capability.

“Over time the cluster will attract further investment, support a growing number of businesses as well as help to develop a dynamic and sophisticated supply chain.”

Creating partnerships
Creating new partnerships between businesses and universities is seen as crucial if the hub is to lead to the successful development and commercialisation of compound semiconductors.

“While we have the core competencies in Wales, part of our vision has to be the creation of a campus like area that will allow much greater collaboration to occur, that’s going to be important for the future success of the cluster,” says Dr Wyn Meredith, Director of the CSC.

“One of our keys aims, as previously mentioned, is to create an extensive and dynamic supply chain. The growth opportunities are enormous and many companies and institutions are already looking to use this technology,” Dr Meredith explains.

Set up in August 2015 as a joint venture between IQE and Cardiff University, the CSC looks to build on research conducted at Cardiff University’s Institute for Compound Semiconductors and to develop innovative new materials technologies to support applications. The Institute is part of a new £300m Innovation Campus at the university.

“The CSC was set up to provide that essential pillar to help span what is called the ‘valley of death’ that exists between industrial innovation and production,” explains Dr Meredith. Shortly after its establishment, the UK Government announced that it would be investing £50m in the CSA Catapult.

CSC is Europe’s first prototyping facility, and is intended to allow businesses and academics to take their ideas and demonstrate new technologies using compound semiconductor materials that will be production ready.

“When we established the centre it was seen as a really strong statement of intent,” said Dr Meredith. “It’s going to be about real projects, real innovation, growth, and jobs in South Wales and we are already involved in a number of new projects.”

If this cluster works then it could not only lift the Welsh economy but the broader economy in general.

According to Dr Meredith: “The CSC gives Cardiff University a clear route to the commercialisation of the research carried out at the Institute for Compound Semiconductors, while for IQE it provide technologies that it can take and commercialise.”

Critics have often pointed to a lack of long-term vision in the UK, but could the approach being taken by CS Connected provide a blueprint for the development of hot technology spots elsewhere in the UK?

A century ago Welsh coal helped to power the industrial revolution, could we see that achievement being replicated, but this time with compound semiconductors powering the next technological revolution?

Above: The Newport Wafer Fab will provide volume manufacturing facilities for the cluster in South Wales

“There are plenty of skilled workers at the Newport facility. We are well placed to contribute to the rapidly developing cluster of companies in South Wales.”

Sam Evans
The Formula E Venturi team has adopted the latest range of ROHM power modules in full SiC technology for its electric-powered racing cars. ROHM has enabled the broad implementation of e-mobility by delivering the next generation of power semiconductor devices. Our modules are produced in-house using a vertically integrated manufacturing system, guaranteeing high quality and a consistent supply to the market.

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At a time when data are fast becoming the most important asset in many organisations there is a growing need for displays. With vast amounts of data helping to determine operational and business decisions, it’s vital that users are able to easily access data and visually monitor sensor readings generated across all types of applications.

So when it comes to developing a display based system, what are the critical elements that should be taken into account?

One of the most important is CPU choice. It is the brain of the entire module, driving all the I/O peripherals, display and touchscreen, or at the very least, is responsible for creating the data that is presented.

In an IoT system, its role is to join the I to the T, connecting ‘Things’ to the Internet and providing content for the local display.

Processors tend to be supplied as a complete Single Board Computer (SBC) or as a stripped down core module (COM).

The choice of processor, and the format in which it is delivered, are going to be key decisions. So, what factors do you need to consider when choosing between SBC and COM options and what are the key specifications to look out for? Finally, what design support will you need?

COM v SBC

Choosing between an SBC and a COM will usually mean a trade-off between time to market and flexibility.

A SBC is a ready to go instant platform that ships with all the drivers needed in the form of a board support package (BSP). It will have fixed computing, memory, and I/O sections integrated onto a single PCB.

A COM or system on module (SOM) is half-way between an SBC and a discrete microprocessor IC. It offers more flexibility than an SBC, but without the development effort associated with a discrete solution. The COM will contain the processor and memory and is then mounted on a separate carrier PCB containing the I/O section of the design.

Clearly, using a SBC saves a lot of integration effort and development time. It comes out of the box as a fully working solution that just needs to be loaded with the application software and interfaced to the display. Problems usually arise when it comes to size and I/O. Each manufacturer offers a limited range of SBC options with different and fixed permutations of I/Os, size and features.

So it is a matter of selecting the most suitable option from the range — you can’t customise the board in accordance with the needs of the application. If a key interface is lacking, then it is sometimes possible to create an adaptor, using the pin header frequently provided. If the board won’t fit into the system caseworks, well, that’s generally a deal breaker.

The advantage of the COM is that you can design the carrier board exactly according to your size and configuration requirements, and then connect an SoM to it. This will take time and design effort, but will allow you to create a board with exactly the I/O that you need for your design and of the right form-factor.

Don’t dismay over display

When it comes to developing display-based systems just what are the key considerations? Rhett Evans explains
Choosing a supplier

Having drawn up a shortlist of boards that tick the technical boxes, it is well worth taking a hard look at the organisation you’re sourcing the board from.

What constitutes a good supplier? They can make a huge difference to your time to market. So always consider the following:

- What is the pedigree of the manufacturer of the board? Do they have a reputation for producing quality, stable products? What long term availability guarantees do they offer?
- Is there a board support package for your chosen operating system? Does it contain all the drivers that you need? Have they been properly tested to work together?
- What is the technical support like? Where is it located?
- Is there a local representative able to support you? How knowledgeable are they?
- How well does technical support know the specific board that you’ll be working with and are they familiar with other key system components like the display? Have they performed the similar integrations in the past?

How good is the documentation? A great question this one – a well-documented design is often a sign of quality.

Does the vendor or the local representative offer value added services?

What is the tool support like? Are there debugging tools available and what is the cost?

That list highlights the need to work with a quality industrial vendor. While you can have fun with a well-known hobbyist platform, if you apply the above tests, then it becomes clear that they are not a sound basis for professional embedded systems development.

A community isn’t a substitute for expert professional technical support, and is your organisation happy to expose aspects of their product development online when you post questions to the community?

In conclusion

When it comes to selecting a processor, the choice will usually boil down to balancing just three key factors: processor performance and specifications; format: SBC or COM (not all processors are available in both of course); and finally, the supplier and the support they can offer.

Selecting the optimal processor but working with a supplier who isn’t willing or able to help you with the design issues you’ll encounter on your journey can significantly lengthen your time to market and even put the success of the project in jeopardy.

So take some time to assess, so you get it right first time round.
Design considerations

As the trend for the Internet of Things (IoT) accelerates with the number of connected devices surges, the demand for IoT gateways has also increased and is forecast to continue to grow exponentially.

The global IoT gateway market is set to grow at a rate of 30.9% between 2017 and 2023 (according to a research report ‘IoT Node and Gateway Market by Hardware, by End-Use, and Geography-Global Forecast to 2023’ by Markets and Markets).

The need for IoT gateways is realised because isolated systems are rapidly transforming to the ubiquitous Internet-enabled system (also known as ‘connected devices’) that can be used to capture and communicate information by leveraging diverse wireless connectivity technologies to IoT gateways for unified edge-analytics.

In other words, IoT gateways play a vital role by providing the fundamental building blocks to develop secure and powerful wireless connectivity between IoT devices and IoT Cloud based applications.

Gateway/hub

As more OEMs look at offering a gateway/hub to connect their existing wireless devices portfolio they have to take into consideration a number of issues.

The main three are: the cost; overall efficiency and effectiveness of the system; and the flexibility that it provides to enable the design of customised IoT solutions that evolve over time.

Typically, when it comes to designing IoT gateways, most OEMs would tend to have taken one of four approaches:

- **Design from scratch** – Building a gateway from scratch based on IoT use case specific requirements with a desired form factor, wireless connectivity and other configurations. While it may have its advantages, this approach tends to increase costs and time to market.

- **Open platform based solutions** – Leveraging open platform-based solutions such as Raspberry Pi, Arduino, or the Beaglebone, and implementing a customised gateway product without extensive programming. This tends to be more suitable for small IoT applications, but isn’t sustainable for larger-scale IoT applications.

- **Fixed configuration-based OEM solution** – Purchase a production-ready gateway platform and then build an IoT application. Most vendors will have fixed configuration and form factor designs and, as a result, do not provide the flexibility to customise the architecture for specific needs.

- **Modular/configurable OEM Gateway solution** – A growing number of vendors such as Phytec, VOLANSYS, Digi, are able to provide a production-ready IoT gateway starter kit platform to build an IoT solution. These can be quickly customised with a modular architecture implementation.

This white-labelled gateway solution is suitable for both small and large scale IoT applications as it is able to provide a flexible architecture and enables faster time to market.

The first three approaches bring a number of issues which may affect a
business, whether that’s in terms of cost-effectiveness or time-efficiency. The fourth one however, provides a middle-ground approach which is both flexible and the most feasible option to prototype custom configurations-based gateways, allowing early field-trials and, more importantly, supporting mass production at reduced time, cost and risk.

So, what are the key factors that need to be considered across an IoT gateway product development lifecycle from prototype to production.

**Prototype design**

While designing gateway prototype platforms, there are several areas like form factor design, hardware platform, wireless connectivity and pre-compliance that will need to be considered whether you are building from scratch or leveraging available platforms.

**Form Factor Design:** IoT gateways combining all functions, such as networking, control and data, security, remote operation and centralised management, are generally forced to compromise on size and form factor over fan-less and vent-less designs.

**Hardware Platform:** For most platforms, the silicon boards; pinouts; and connectors are not friendly enough for using the platform to test the market. Traditional prototype designs are not compatible with a diverse range of peripherals that restrict the use of gateways in multiple applications.

**Wireless Connectivity:** Most of the prototype ready gateways that are currently available offer limited options for wired and wireless connectivity using standards such as Zigbee, Wi-Fi, LTE, Thread, Z-Wave, Sub-GHz RF, where some of these may not be available as an option.

Also, providing more options for both southbound and northbound connectivity increases the time to market. Solutions that allow product developers to choose from the northbound interface (Wi-Fi, LTE, Ethernet) and southbound interface (Zigbee, Z-wave, LoRaWAN, Sub-GHz) tend to be very rare.

**Pre-Compliance:** The most critical phase is to get the gateway certified before it is made available in the market, because of the time-consuming certification processes. So, pre-compliance considerations need to be addressed in good time. In today’s market, certification ready platforms can help to reduce by up to three months the PDLC prior to product launch. Designers need to be aware that the total time for such products to hit the market will increase significantly if the platform is not pre-certified. At present, there are very few gateways available in the market, which provide FCC/CE/IC pre-certification along with multiple connectivity options like Zigbee, Thread, Wi-Fi/3G, and Bluetooth.

**Key factors**

So OEMs face multiple challenges when it comes to preparing their gateway prototype design for high-volume production. To avoid these challenges, some OEMs might consider selecting a production-ready platform for their gateway requirement.

As a result there are a few factors that OEMs will need to consider for high-volume gateway production. These include:

**NRE charges:** If the gateway prototype platform does not meet the defined product requirements of OEMs before they ship the first unit after production, high NRE charges may impact profits due to lack of pre-planning around tooling enclosures, certifications and MOQ of purchases. The total production cost increases mainly because of custom-made products, and divert engineering and production resources from standard, consistent product lines, over to one-off designs with little opportunity to recoup design costs through large-scale production.

**High Volume Supply:** In many markets 10K is a small volume to be supplied per year. It restricts some players who try to innovate the end-application as the addition of R&D time, prototype development time, production time and time to test the market for an application, increase the total time to launch.

**Support for Chip Down or Product Enhancements:** A thoughtful product prototype design can be accomplished with a well-architected gateway that is production-ready, and that fulfills all the critical product requirements. After initial customer trials when production reaches certain volumes, the product should be converted to chip down versions to support large volumes.

During the IoT gateway product development roadmap from prototype to production, OEMs will always face numerous compromises when it comes to one or the other factors described here. As designing and creating IoT devices is never easy, modular IoT gateways, will tend to help add real value to an IoT applications.

Gateways should be a central consideration when planning any IoT architecture and selecting the right one should often be the starting point, as the gateways play a significant role in all facets of IoT – from connectivity management, to monitoring, and data processing, to cloud integration.

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Heart of glass

The encroachment of glass into mainstream production has been slow up till now, but could the push to deliver higher throughput more cheaply see the material have a bigger role to play? By Chris Edwards

For more than half a century, high-purity silicon has dominated the world of IC production. It’s a material that has almost everything. Silicon is not just an effective semiconductor, it is mechanically strong. That is in direct contrast to many of the III-V materials that offer high performance but are much more fragile.

Sapphire provides strength and excellent electrical isolation, but is difficult to integrate into manufacturing economically. As a result, materials such as gallium nitride that are useful in high-brightness LEDs and power devices, have shifted from sapphire to silicon wafers.

A challenger is emerging but even that is based on silicon. Tweaks to the chemistry and manufacturing processes are now making glass a powerful contender.

One advantage that glass has is that it works well as a companion to silicon, making it possible to tune manufacturing processes and experiment with novel ways to eat into adjacent markets.

According to the market analyst firm, Yole Développement, the biggest use of glass as a substrate is in microfluidics and it is likely to stay that way into the early 2020s even as other uses develop for the material.

Although polymers such as polymethyl methacrylate (PMMA) have become popular for lab-on-a-chip devices, because they can be cheaper to process, many applications cannot use them because solvents and reagents are more likely to attack them. Glass and pure silicon are far less likely to react.

Glass carriers

The other major use of glass today is largely hidden away. Ever since ICs were incorporated into smartcards, fabs have had to find ways to keep silicon wafers stable and flat while they etch away at the underside and then attach interconnect to the top. As it is thinned down to just a thickness of 100µm, silicon easily bends and sags. The answer is to temporarily bond the thinned wafer to a glass carrier.

One big advantage of using glass as a carrier and substrate is that subtle changes to chemical composition make it possible to match the thermal coefficient of expansion (CTE) to whatever it needs to be bonded. This, in turn, is likely to see glass move from the fab into the IC packages themselves.

At the start of the decade, Georgia Tech’s Packaging Research Center started to look at using glass inside the 2.5D and 3D multichip modules that had begun to appear in high-density smartphones, high-end networking equipment and computers.

For 2.5D and 3D packages, manufacturers were faced with two distinct choices. The first, was to adapt the existing organic-polymer materials used for low-cost IC packages to work as mini-PCBs that interconnect the multiple chips inside the module. The organic materials, however, have two problems. Although they are cheap to use, there are limits on how dense the interconnect can be. Organic packages tend to suffer from warping and stretching when heated and cooled, which can cause very thin connections to bend and then break completely. As a result, there are limits on how thin and how closely spaced interconnect traces can be, which makes it difficult to design modules that need very wide buses between devices inside the package.

The other option pursued by chipmakers up till now at a
commercial level is to use silicon as an interposer. Foundries such as TSMC have redeployed older fab lines, typically those capable of producing 90nm or 65nm-generation ICs, to make interposers with an interconnect density that rivals that found on the chips themselves, albeit at higher cost. The interposers are generally entirely passive although there is potential to put switches and other active devices onto the substrate.

Georgia Tech’s PRC proposed glass as a third option that can rival the interconnect density of silicon and greater CTE compatibility but with a cost structure closer to that of organic packages. Unlike silicon, the glass does not have to be made in wafer form. Experience with LCD manufacture has led to a mature market for equipment that handles large rectangular panels. This allows more devices to be handled at a time and without the waste of cutting square devices out of a circular blank. Glass suppliers have demonstrated the ability to form substrates that measure 1m on a side, although 500mm looks likely to become a common size for packaging work.

A further advantage of glass is that it remains mechanically strong even when thinned in the same way as silicon. Even roll-to-roll processing is possible thanks to the way glass becomes much more flexible when thinned to extreme levels. The researchers have worked on interposers that are as thin as 50µm to support low-profile packages.

**Brittleness a problem**

But they found it was not all good news for glass. The legendary brittleness of glass and its low thermal conductivity could prove problematic. Chips are often designed with the notion that a large proportion of the heat they produce will escape into the PCB. Designers would have to rethink this if their devices were flip-chip bonded onto a glass substrate.

A technology devised to increase interconnect density in 3D packages may yet help glass become the interposer of choice by helping to deal with its problems. Through-silicon vias (TSVs) have made it possible to build dense stacks of DRAM that deliver much higher throughput than conventional memory modules. The process involves drilling or etching holes in the substrate and filling the cavity with copper or a similar conductor to connect traces from the top to the bottom surface of each device in the stack.

Through vias on organic laminates cannot be spaced much closer together than 200µm. TSVs can be spaced as close together as 10µm, though most designs will use a more relaxed pitch because the relatively thick copper traces can easily eat into space on the die that needs to be used for active logic. Work by the PRC as well as suppliers such as Corning has produced test devices on glass with through vias spaced 30µm apart.

The copper conductors could help with both the problems of fragility and thermal conductivity. The metal vias will help convey heat more efficiently to the PCB. R&D teams have proposed using additional copper structures. In dense stacks, the copper could convey heat to spreaders around the edges of the package. Corning also found the thinned glass is less likely to break in areas that contain vias.

**Wireless applications**

Although high density could see glass begin to displace organic and silicon interposers in computing-oriented products, other properties of glass point to the early applications being in wireless communications. Glass is already used for making passive RF filters and similar devices, and has advantages in RF interconnect. The Industrial Technology Research Institute (ITRI) in Taiwan has tested interconnects useful for RF work at up to 20GHz. The group found lower losses in glass-based waveguides and microstrip lines compared to silicon substrates.

Its high resistivity favours the use of glass as a medium for carrying integrated passives that operate at the frequencies needed for 5G and millimetre-wave radio.

STMicroelectronics set up lines to make integrated passives on glass several years ago. Work by Corning and Qualcomm has looked at building high-Q inductors on glass using metal-insulator-metal architectures. The ability to pack many passives together underneath an SoC may also help see glass adopted for high-density IoT controllers.

The encroachment of glass into mainstream production has been slow up till now and almost invisible. But the push to deliver higher throughput more cheaply may see the material become a much bigger player in the coming decade.
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The much discussed Industry 4.0 takes the automation of the manufacturing process to the next level, with the focus moving from mechanisation and mass production to the decentralisation of the control and regulation of the production process.

This, combined with a move away from the traditional hierarchical communication structures seen in production, has given rise to a new networked model.

“Whilst production automation is currently controlled ‘top-down’, in future we’ll see a much more distributed model,” suggests Mark Ellins, Senior Director, Custom & Enterprise Solution BU, Socionext.

Ellins says that the networking of the various elements that make up the production process will be possible and will help to optimise the entire value-add chain.

“The possibility of each node being able to communicate with others will enable local decision-making and increased efficiency,” says Ellins.

A basic principle associated with Industry 4.0 is the ability it affords those authorised operators to directly access the individual nodes via the Cloud, independent of their physical location.

“This will influence the overall production process,” Ellins explains, but that will mean that, “the security of the system will have to be guaranteed. Data Security is an important issue for Industry 4.0. The potential for misuse or external influence is extremely high and security is a key topic.”

Socionext designs, develops and delivers System-on-Chip (SoC) products.

“Our focus is on imaging, networking and computing all of which drive today’s leading-edge applications and, as a business, we have been focused on Industry 4.0 for a long time, working with a long list of customers in this space,” explains Ellins.

“There are a number of key challenges within Industry 4.0 from networking and data handling to supporting new applications such as machine vision, and our focus on computing, networking and imaging matches well with what we are currently seeing in the smart factory space.”

Ellins makes the point that when it comes to the adoption of Industry 4.0, “We’ll have to accept that it constitutes a major structural change in the way in which business will be conducted. While it is being adopted by larger manufacturers, and by companies operating in specialist areas, I believe we’ll see a growing number of SMEs adopting those aspects that are most relevant to their needs.”

According to Ellins, the ability to process vast amounts of data at the Edge is becoming increasingly important.

“While we’re seeing growing demand for computing and networking capabilities on the vision and imaging side, image recognition without human intervention, is becoming more important. We’re working closely with companies who specialise in AI, as a result.”

Challenges abound

Real-time capability is particularly important at the production level. Inputs from sensor values must be processed within defined timescales and this has resulted in new sets of requirements for data transmission and processing.

A further challenge with the implementation of Industry 4.0, according to Ellins, is the large number of communication standards which have been adopted within the production environment.

Crucially, both reliability and functional safety of the individual equipment in use are becoming essential, and in order to reduce servicing requirements for Industry
4.0 components, high Mean Time Between Failure values are now becoming mandatory.

“Functional Safety is of particular importance for production processes where failures could lead to physical risk to the operators,” Ellins suggests.

It is clear, that Industry 4.0 involves a much higher investment in both electronic systems and the supporting IT infrastructure.

The networking of all the individual system components places demands on both hardware and software that require new approaches and ideas.

As Ellins suggests, it has been a subject of focus within Socionext for some time and the company has developed a number of semiconductor solutions which simplify the development and support of Industry 4.0 equipment.

Interestingly, this is particularly relevant when it comes to the company’s Application Specific Integrated Circuits (ASIC) business unit, where a variety of new solutions for applications have been developed.

ASICs are seen as playing a key role in the provision of optimised IC solutions, according to Ellins.

“Industry 4.0, with its special requirements, is an area where ASICs can bring many advantages. These devices are very valuable for a number of reasons, including differentiation and IP protection, which is becoming increasingly important and security. Security of the systems used to support Industry 4.0 is the biggest challenge we face today and we believe that it is better covered by using an ASIC,”

Using ASICs means that customers can develop proprietary logic solutions and have full control over the functionality of the final device.

“Optimised package solutions can be chosen based on the specific requirements of the operating environment and power consumption,” according to Ellins.

Besides the possibility to implement proprietary logic solutions and functionality, the developer can, as part of the ASIC design, take advantage of a large number of per-configured functions such as processors, analogue function such as A/D converters, SRAM or Flash memory.

“We are also able to offer dedicated IP functions which have been optimised for Industry 4.0 applications. One example is our Secure Ethernet Processor IP which enables data communication at rates up to 1Gbps.”

Functional Safety requirements are also covered. For example, loss of clock signals can be monitored by a dedicated on-chip module in order to force the chip into a special fail-safe mode. On the chip reliability side, on-chip sensors can be used to monitor data such as die temperature or power consumption in order to track the device’s aging process and predict failures before they occur.

“ASICs are associated with a higher level of development effort in comparison to discrete solutions, so an ASIC development is probably better suited for higher-volume equipment,” concedes Ellins.

For computing applications, Socionext has developed its Platform SoC family (MB86S7x) of general-purpose ARM-based processors. These devices are intended for complex applications, as in addition to the main processor they also integrate a powerful graphics processor (GPU), as well as a variety of external interface options.

Socionext’s SynQuacer offers a multiprocessor solution with 24 ARM A57 cores.

“This is an extremely powerful processor that has been designed to enable new AI applications in areas such as Machine Vision and Big Data,” Ellins explains.

A key requirement of Industry 4.0 is real-time capability across all network nodes, and Socionext has developed an Industrial Ethernet Processor (IEP) that supports two MII/GMII ports for connection to external Ethernet PHYs, allowing the daisy-chaining of network nodes – a common requirement for industrial applications.

The IEP supports several current Industrial Ethernet protocols. It checks received frames and can automatically decide whether these should be stored, processed or forwarded. With its integrated Quality of Service (QoS) engine, the IEP is also able to support the emerging Time-Sensitive Network (TSN) protocol, enabling the transfer of data within guaranteed timeframes as demanded by real-time applications.

Simple control systems can be easily implemented with the IEP. Since the IEP (in addition to its two Ethernet ports) also supports other bus standards, such as I2C and SPI, external devices like displays and sensors can be controlled directly.

More complex solutions can be implemented by connecting the IEP to an external processor and the IEP is also available as an IP block for integration into a larger ASIC solution.

The transition to Industry 4.0 is certainly gathering pace, but it is continuing to throw up many design challenges which suppliers will have to work hard to address.
The need for machine learning in systems that have to operate safely, means that researchers require a better understanding of how these technologies work and how they make mistakes. By Chris Edwards

Momentary lapses of reason

More than a decade ago, when the idea of self-driving cars still seemed a long way from reality, an experiment revealed how odd machine-made decisions can seem to the casual observer.

In the Urban Challenge competition organised by US research agency, DARPA, two autonomous vehicles collided at low speed in a way that, at first, baffled the designers.

Cornell University’s Skynet had trouble with its software and slowed almost to a halt – but not completely. It was still lurching forward intermittently. Approaching from behind, MIT’s Talos considered everything moving below a certain speed to be effectively static and cut in front – just at the point Skynet lurched forward again, this time hitting Talos.

More than a decade on, a misclassification problem looks to have played a major role in the death of a cyclist that crossed a dark road in Arizona in front of one of Uber’s experimental self-driving cars. The information reported anonymous sources who claimed the car’s software registered an object in front of the vehicle, but treated it in the same way it would a plastic bag or tumbleweed carried on the wind.

Autonomous vehicles have to make split-second decisions based on how they classify the objects in the scene in front of them.

Developers currently favour using AI techniques because purely algorithmic methods are likely to be too complex to develop. But when AI makes mistakes, working out why becomes the problem. It is an issue that extends way beyond self-driving vehicles.

Pinning down the misclassification to a flaw in the training data or the structure of the learning algorithm itself is much harder than understanding that something has gone wrong. Despite the huge amount of R&D money now being poured into deep learning in particular, the ability to validate and verify the systems remains poor.

Researchers regard deep neural networks as being, for the most part, black boxes.

Professor Philipp Slusallek, scientific director at the German Research Centre for AI (DFKI), said in his keynote at CDNLive EMEA 2018: “At the moment, we don’t have any verification technology for deep-learning networks. We don’t yet understand the limits of this technology.”

Rich Caruana, senior researcher at Microsoft Research, says AI today has a core problem: “It’s an idiot savant. It has an incredibly narrow understanding of the world.”

Deep neural networks demonstrate this in the way they sometimes home in on features in an image that are completely different to those used by humans. Often, unconscious choices in training data will give too much significance to elements that, to the machine will seem important, but which are really just the result of coincidences.

A system to classify images as pets might well use the presence of a cardboard box to push the conclusion in the direction of “cat” simply because so many are photographed
at the Data, Learning and Inference Co-Founder and CTO, Amnon Shashua, powered car unacceptable. Mobileye in the real world and make the AI-the user acceptance of systems no human would.”

“Imagine you are driving a car and the car suddenly brakes for no apparent reason. You will take the car back to the dealership. We are talking about designing things that have to show zero false positives. If you go to fully autonomous driving it gets even worse.”

There are other problems besides braking or not braking at the wrong times. Shashua points out autonomous cars will need to work out how to handle tasks such as merging onto busy motorways – and understand when other drivers will make space for them – or be left stranded at the side of the road. Making the robot understand the subtle behavioural and environmental clues that affect real-world driving will take much more work, due to the way neural networks currently operate.

“Deep learning needs lots and lots of data,” says Slusallek. It could take millions of miles of real-world testing to reveal enough combinations of conditions to both train and validate the AI’s behaviour. “The only way we can make sure our systems do the right thing is to generate the data synthetically,” Slusallek adds, so that the systems can be tested much more extensively in a virtual space.

XAI programme

Extensive behavioural testing can only go so far. Engineers need to be sure that the system is not interpreting incoming data incorrectly and has simply been lucky in not triggering unwanted reactions. Caruana argues for AI to be explainable, and has pursued research on alternatives to deep learning that are easier to interpret. DARPA is equally keen to find AI systems that are explainable. The XAI programme got underway two years ago and is recruiting researchers from the US and beyond.

Subramanian Ramamoorthy and colleagues from the University of Edinburgh, for example, are working with the Palo Alto Research Center (PARC) on one project under the XAI banner to infer models from analysis of the behaviour of AI systems. Researchers working outside the DARPA programme are pursuing a number of ways to address AI verification. Xiaowei Huang and colleagues from the University of Oxford have worked on formal verification techniques that perturb the network and its input data to determine the stability of classifications made by the network. Runtime performance is a major challenge, but work along these lines should make neural networks more resistant to noise-injection attacks as well as poorly balanced training sets.

Other teams are focusing on supplementing or replacing black-box AI with models that lend themselves more readily to analysis. University of Toronto researcher, Professor Angela Schoellig, is working on coupling programmatic models with machine learning. This should make it possible to start with a system that behaves safely, because it is driven by the physics models, but which gradually incorporates more behaviour that is learned when it performs.

A team from the University of California at Berkeley aims to use a second AI system based on Bayesian learning as a back-up for the more sophisticated deep-learning core. In principle, this would force the robot to make safer choices and not be misled by anomalies in the training.

At such an early stage in the development of dependable AI systems, the way forward remains unclear. But the need for machine learning in systems that are expected to be safe under all conditions is forcing much deeper investigation of how these technologies really work and how they make mistakes.
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Last month Cadence unveiled the latest version of its Virtuoso Platform in a move intended to support enhanced system design and simulation layout. Not only that, it has been enhanced to better support the development of advanced nodes from 22nm down to 5nm.

According to Yuval Shay, Product Management Director, Analog/Custom IC Group, Cadence: “What we have announced is a significant upgrade to the Virtuoso Platform. I don’t think there’s a single application that we haven’t upgraded or made significant changes to.”

The enhancements affect almost every Virtuoso product, providing system engineers with an environment and ecosystem that will enable them to design, implement and analyse complex chips, packages, boards and systems. “The engineering community needs EDA tools that are able to provide them with the ability to efficiently design, test and layout circuits that not only address the issue of reliability but do so without impacting on a designer’s productivity,” Shay explains.

Some of the big challenges facing EDA today include its ability to handle shrinking device/process size and to manufacture those advanced nodes as well as the impact of multi-technology designs and model support of devices and multi-technology simulation.

As Shay suggests, “Today, design teams need to be able to easily and quickly prototype designs and that requires much more agile editing in order to work quickly through design optimisations that use manufactureable parts and processes that can be controlled.”

The latest version of the Virtuoso Platform is a response to that, but is also looking to address one of the biggest challenges confronting companies today.

“Traditional system companies that in the past would not have attempted to design an IC or use Virtuoso, or had a team that specialised in analogue design, are becoming more vertically integrated. As a result they are taking a much more system approach when it comes to bringing products to market. “Likewise, our traditional customers, i.e. semiconductor companies, are developing more integrated solutions and are looking to provide their customers with systems either in the package or on the board – it’s no longer simply about IC design, but system design.

“The level of integration that we are seeing is extremely high, and Virtuoso looks to address this trend,” Shay says.

Shay explains that at the heart of the new system’s design environment is a set of technologies that enable simultaneous edits across multiple process design kits and technologies. “The platform has also been designed to provide seamless interoperability with Cadence’s SIP Layout and the Sigrity analysis technology portfolio for a comprehensive chip-to-board toolset.”

According to Shay: “One of the big challenges confronting design teams is dividing layout tasks. Virtuoso now features a concurrent real-time team design editing capability, which allows teams to distribute layout tasks and perform what-if explorations. This is particularly useful for design-rule check (DRC) fixing, chip finishing and manual routing.”

While every design will be different, Shay takes the example of LIDAR to demonstrate how this platform will benefit, in this case, designers working in the automotive space.

“Lidar is the laser equivalent of radar and works by sending out laser pulses and then timing when they return. By doing that, it is possible to build up a picture of what is surrounding the vehicle,” Shay explains.

But Shay makes the point that at present, “it simply costs too much
to install economically in vehicles. Estimates vary, but if each vehicle needs, say, 15 of these devices the costs are prohibitive. “LIDAR is very mechanical and expensive; we need to see an integrated solid-state solution that costs under $100, and while it’s going that way, it’s clear that it remains at a price point that is unsupportable in all but the most expensive vehicles.”

If the cost of LIDAR is to be reduced, then the way it is made has to be cheaper and that means using solid-state laser diodes, MEMS mirrors to direct the light, silicon photonic detectors, and substituting high-precision optics with lots of digital signal processing.

According to Shay that would require a LIDAR that incorporates a laser-diode transmitter, with MEMS mirrors, a super-sensitive SPAD detector (single photon avalanche diode), and signal processing that is capable of pulling the whole system together.

“There are several different technologies that need to be packaged together,” he says, “and in order to achieve that, design engineers need a system that can handle all of these technologies not just one at a time, but in the context of the packaging, and the other die.

“Throw in Artificial Intelligence and neural networking to look at and process an image, and all of this will take integration and a lot of products.”

Crucially, there is full interoperability between Virtuoso (layout), Allegro (PCB and packaging layout), and Sigrity (signal and power integrity) providing the support necessary for mixed technologies such as MEMS, photonics, power devices, RF, as well as mainstream analogue and digital silicon.

**Advanced nodes**

In this release of the Virtuoso platform, Cadence has also incorporated innovative advanced-node methodologies that speed the designs done in process technologies from 22nm down to 5nm.

“Many companies are using these advanced nodes, many more than we anticipated,” says Shay.

“While there’s demand for older nodes we need to provide a solution for 5nm designs; there are more than 170 companies developing in advanced nodes – the growth has been amazing. In automotive for example, we are seeing products using 16nm and 7nm.”

By collaborating with leading-edge foundries, ecosystem partners and customers, Cadence has been able to develop advanced technologies that are able to automatically manage process complexities with innovative methodologies that allow engineers to focus on their designs.

In circuit design and analysis, advanced statistical algorithms specifically targeting FinFET designs are able to uncover circuit variances early on in the design process, reducing design variation analysis time by as much as 20% using advanced statistical algorithms.

In layout design, a unique multi-grid system abstracts complex design rules of the latest 7nm and 5nm processes, while allowing engineers to increase their use of placement and routing technologies to significantly increase their layout design productivity.

“The Virtuoso Layout environment is evolving from an electrically aware layout to the industry’s first electrically and simulation-driven layout using unique sets of in-design technologies to ensure circuit integrity and performance,” Shay suggests.

This new simulation-driven layout addresses many of the electromigration (EM) and parasitic challenges of critical circuits and advanced-node designs.

To increase layout automation, the new environment has introduced several techniques for hierarchical floor-planning and planning, along with new placement and routing automation technologies to increase layout design productivity and throughput, and to shorten layout turnaround time.

“We estimate that this layout environment with electrically driven routing and wire editing, real-time design editing, and revolutionary design planning techniques will help to improve productivity by up to 50 per cent,” according to Shay.

“In this market, the winners will be those companies that evolve the fastest - they’re not always the smartest or the richest, but those that re-tool around these new trends and address them the fastest,” Shay concludes.
Mouser Electronics Signs to Global Distribution

Mouser Electronics Signs Advanced Energy Industries to Global Distribution Partnership

A global distribution partnership with Advanced Energy Industries (AEI), a global leader in precision power conversion. Through the agreement, Mouser will stock AEI’s power portfolio, including high-voltage and thermal products.

“This partnership with Advanced Energy bolsters our commitment to providing the latest products and technologies to our customers worldwide,” said Jeff Newell, Mouser Electronics’ Senior Vice President of Products. “We look forward to providing engineers and buyers worldwide with AEI’s innovative power solutions, backed by Mouser’s unsurpassed customer service and best-in-class logistics.”

To learn more, visit www.mouser.com/advanced-energy.

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Red Pitaya adds Vector Network

Analyzer capabilities to low cost credit-card-sized, reconfigurable STEMlab instrument

Multi-function, open-source, reconfigurable test & measurement platform can now measure electrical performance of RF components

Red Pitaya, the company that is pioneering the move to low cost, open-source, reconfigurable instrumentation with its credit-card-sized STEMlab® platform, today launched a VNA new bridge module and application that enables STEMLab to function an affordable vector network analyser (VNA), a precision measuring tool that tests the electrical performance of high frequency components in the radio frequency.

STEMlab is a test and measurement environment that includes a board, an application marketplace and a source code library. It is designed as a low-cost alternative to many expensive measurement and control instruments. STEMlab can function as an Oscilloscope, Logic Analyser, Signal Generator, Spectrum Analyser and more, also performing other tasks, now including vector network analysis.

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Taiwanese opens new facility in UK

LED giant Ledtech opens new facility in UK

Ledtech, one of the world’s largest capacity LED manufacturers, has announced the opening of a European facility in the UK.

The addition of a direct facility adds a range of value-added manufacturing services, design in support, volume availability and security of supply on a wide range of opto parts including discrete LEDs, LED displays, lighting components and luminaires. Additionally, later this year, the company will install a full LED production line in the UK facility.

Key markets include commercial, consumer, industrial, office, retail, business & finance, transportation, signage, instrumentation, healthcare, vending & gaming machines, hotels, restaurants & leisure and public spaces.

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Ultra-Low Power Lattice sensAI

Mass Market Enablement of Artificial Intelligence in Edge Devices

New FPGA Solutions Open Doors for Rapid Deployment of Machine Learning Inference Across Broad Market IoT Applications Demanding Milliwatt Range Power Consumption

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Full-featured Lattice sensAI stack offers modular hardware platforms, neural network IP cores, software tools, reference designs, and custom solutions via partner eco-system.

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EDT Smart Embedded Products

New modules enable the user to add a modern GUI with High-end graphics and smooth animation to any system without the overhead of a memory and power hungry operating system.

The controller board is integrated with the display as one compact module. It includes all necessary circuits to control the TFI module, backlight, PCAP and the Dig application.

The graphical framework is based on Touch GX and FreeRTOS. Three modules are available – 4.3 inches, 7 inches & 10.1 inches.

Evaluation kits are also available.

For you tube video see: https://www.youtube.com/watch?v=cm8ShyJq0QM
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OKW EVOTEC enclosures now in four sizes

OKW’s EVOTEC designer electronic enclosures are now available in a new smaller 100 size

OKW’s EVOTEC designer electronic enclosures are now available in a new smaller 100 size – increasing the range to four plan sizes. There are two versions: with a flat top or with a 32° inclined top for an improved viewing angle.

Screw pillars are provided inside for installing PCBs. The Torx® assembly screws prevent tampering. EVOTEC’s soft contours are moulded from UV-stable plastic in off white [RAL 9002] Accessories include an IP 65 sealing kit, wall mounting kit and PCB fixing screws.

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SCALE Gate Drivers Now Available

Power Integrations’ SCALE Gate Drivers Now Available with Conformal Coating

Enhances robustness in harsh environments; streamlines manufacturing logistics

Power Integrations [Nasdaq: POWI], the leader in gate-driver technology for medium- and high-voltage inverter applications, today introduced factory conformal coating for its SCALE™ EGB and MOSFET drivers. Conformal coating enhances system reliability by protecting electronic components against contaminants such as pollution, dust and condensation, which may cause corrosion. Power Integrations’ factory-coated gate drivers reduce inventory cost, lead time and overall cost of ownership by eliminating the need for manufacturers to send boards to subcontractors for cleaning and coating.

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TTL, Inc. announces winners of 2017

TTL, Inc. drives continuous improvement in customer service and announces winners of 2017 Supplier Excellence Awards

AX, Burums, KEMET, KoaM, Moles, Murata, Vishay & Yageo featured in TTL’s 2017 honours roll call

TTL inc., world-leading specialist distributor of electronic components, has named this year’s winners in its Supplier Excellence Awards programme, acknowledged across the industry as a rigorously audited and highly sought-after recognition of quality performance. Throughout the year, TTL measures performance against specific actions – including on-time delivery, administrative quality, operations and business systems and joint customer support – and awards points according to challenging quality performance standards.

Photo Caption: KEMET won TTL’s Global Operations Excellence Award.

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