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Comment

Things can only get better....

As the global economy slows so the on-going US/China trade war enters a new phase

The latest PMI figures, both here in the UK and Europe, are pointing to a sharp slowdown in factory output. New orders are falling and, in the case of the UK, activity is sliding at its fastest pace since 2012.

Europe’s factory sector has been contracting for seven months and Germany, in particular, is showing increased signs of economic stress due to the slump in global demand for both cars and machinery.

While these figures reflect a wider slowdown in the global economy and the UK is having to contend with the ‘economic and political uncertainty’ that surrounds Brexit, the on-going US-China trade war, further exacerbated by the Trump Administration’s decision to extend tariffs on billions of dollars of additional imports from China, is now starting to seriously impact the electronics industry.

From the start of this month TV, drone or smart speaker imports from China, for example, will now attract a 15% tax, even Apple AirPods and Watches will now be affected.

According to Bronwyn Flores, a spokeswoman for the Consumer Tech Association in the US, a trade body that represents upwards of 2000 companies in the electronics industry, “prices are likely to start to increase this holiday season,” in the US.

Since July 2018 tariffs have cost the US electronics industry, and its suppliers, upwards of $10billion – mainly in terms of parts and components. These latest tariffs, however, are likely to start impacting finished goods.

“List 4A”, which is a list of tariffs that have just come into effect will impact devices from smart watches to lithium batteries and are expected to affect upwards of $50billion worth of consumer goods.

Leading companies like Apple are expected to absorb the additional costs but with further tariffs “List 4B” scheduled to come into effect in December and impacting smartphones, tablets and video games consoles, you have to ask how much longer can companies, even the likes of Apple, avoid passing those costs on to consumers?

Companies will be able to apply for exemptions but when the list of recession signals are flashing red this is just adding to uncertainty and to fears of an economic slowdown.

The prospects aren’t great then as we approach 2020.

Sluggish economic growth and potential currency devaluations are coinciding with a trade war that continues to weigh heavily on business confidence and is, according to a growing number of analysts, unlikely to end any time soon.
YOU

We Make
A broad range of systems continue to employ increasing numbers of advanced SoC (System on Chip), FPGA, and microprocessor solutions. Each successive generation expands in power budget as power-hungry components are added and data processing speeds rise to support live streams of telecom, audio, or video data.

These demands can only be met by robust, easy to use low voltage power supplies with high efficiency, high power density, and low electromagnetic radiation.

SoCs and FPGAs require a number of low voltage supplies, including 1.1V for DDR, 0.8V for core, and 3.3V/1.8V for I/O devices. Delivering sub-1V will usually require two stages: an intermediate regulation stage to 12V or 5V, and another to low voltage. Each dc-to-dc conversion must be efficient and pass EMI standards to enable the overall power system to perform efficiently.

It can be difficult to meet size, efficiency, and EMI design goals using conventional buck regulators. Sub-1V buck regulators traditionally rely on bulky and EMI noisy PWM controllers and MOSFETs. The demands of automotive and industrial systems mean that devices must give way to something more compact, with higher current capability, higher efficiency, and superior EMI performance.

Monolithic Silent Switcher 2 buck regulators in the LTC7150S and LT8642S family have been designed to address these SoC power demands.

EMI performance
EMI issues that crop up in the late phase of the design and development of a system can cost significant money and time in troubleshooting and redesign. So, to assure EMI qualification throughout the power supply design process, EMI suppression is often prioritised, and sometimes over-engineered, at the expense of other desirable features - namely efficiency, reliability, and simplicity.

EMI usually involves slowing down switching edges and/or lowering switching frequency. However, this can come with significant trade-offs, including increased minimum on-times, limited voltage conversion ratios, and larger solution size. Alternative mitigation techniques, such as bulky EMI filters or metal shielding, add significant costs in board space, an increased component count, and greater assembly complexity.

None of these strategies meet the requirements of the demanding SoC power budgets of compact size, high efficiency, and low EMI.
The LT8642S is an 18 V/10A step-down monolithic Silent Switcher 2 regulator in a 4 mm × 4 mm LQFN package. With only a ferrite bead and input capacitor as the input EMI filter, it is able to meet the stringent CISPR 25 Class 5 radiated EMI specification with abundant margin. Another popular EMI specification is CISPR 32 often used by consumer electronics manufacturers. LT8642S can easily meet the CISPR 32 Class B radiated EMI specification even without the input EMI filter.

The LTC7150S is the first of its kind, a 20A, high efficiency step-down regulator with Silent Switcher 2 technology incorporated to minimise the electrical magnetic emission, which greatly simplifies the EMI filter design and layout. The Silent Switcher 2 architecture brings in exceptional EMI performance while minimising the ac switching losses in monolithic regulators. Hot loop capacitors are included in the IC significantly reducing noisy antenna size and minimises EMI.

Switching node ringing is minimised on the very fast switch edges, reducing high frequency noise, and associated energy stored in the hot loop. Also, the hot loop is split in two and symmetrically laid out for EMI self-cancellation. This yields quiet power for the noise-sensitive automotive environments, where powerful SoCs are employed for advanced drive assistance systems (ADAS) or autonomous drive systems. This also satisfies the requirements of telecom, transportation, and industrial systems, where high efficiency, low noise power supplies are needed to power the next generation SoCs, CPUs, and microprocessors.

LTC7150S passes the CISPR 25 radiated EMI peak limit with a simple EMI filter installed in the front.

**Expanding output current**

Advanced functions such as autonomous drive and self-parking demand more powerful SoCs to implement live stream visuals or artificial intelligence. For processor systems that demand more than...
20A current capability, multiple LTC7150Ss can be paralleled and run out-of-phase.

The LTC7150S features a sync function that enables synchronisation to an external clock, and the internal PLL (phase-locked loop) allows the LTC7150S to be operated out-of-phase for multichannel, multiphase operation to reduce ripple.

The CLKOUT signal can be connected to the MODE/SYNC pin of a following LTC7150S to line up both the frequency and the phase of the entire system. Multiphase operation is implemented at the PHMODE pin.

Tying the PHMODE pin to INTVCC, SGND, or floating the pin generates a phase difference between the clock applied on the MODE/SYNC pin and CLKOUT; differences of 180°, 120°, or 90°, respectively, corresponding to 2-phase, 3-phase, or 4-phase operation. A total of 12 channels can be run out-of-phase with respect to each other by programming the PHMODE pin of each LTC7150S to different voltage levels.

Figure 1 (previous page) shows two converters connected in parallel to provide 40A output current at 1.2V. The clock from the master unit is synced to the slave unit by tying the CLKOUT of U1 to the MODE/SYNC of U2.

The master PHMODE pin is tied to ground, and the slave PHMODE pin is left floating. This results in 180° phase difference between the two channels, reducing the input current ripple.

To ensure better current sharing in steady state and during startup, ITH, FB, and TRACK/SS are tied together. Local RT resistors are needed and should not be tied together. Kelvin connection is recommended for accurate feedback and noise immunity. Place as many power vias as possible in the vicinity of the ground pins to the bottom layer to improve the thermal performance. Ceramic caps of the input hot loops should be placed close to the VIN pins.

The inductor current is balanced during startup and steady state as shown in Figure 2. Efficiency can be as high as 89% at 32 A, when the input is 3.3 V.

The LT8642S also features enable control, a power good indicator, and soft-start. These functions are essential to the system power sequencing, required by SoC and FPGA power supplies.

ADI’s Power by Linear portfolio offers a range of buck regulators to fulfill the wide-ranging power budgets of advanced SoCs, FPGAs, and microprocessors.

Conclusion

The demand for more intelligence, automation, and sensing has resulted in a proliferation of electronic systems that require increasingly high-performance power supplies. Low EMI has risen from afterthought to top priority, while solution size, high efficiency, thermal proficiency, robustness, and ease-of-use remain important.

ADI monolithic regulators look to satisfy the requirements of automotive, telecom, data centre and industry customers. In particular, the family of high-performance monolithic regulators that includes the LTC7150S and LT8642S meets stringent EMI standards in a compact size by incorporating proprietary Silent Switcher technology.

Integrated MOSFETs and integrated thermal management features enable robust and reliable delivery of current from several amperes to beyond 20A from input ranges up to 20V and with control, power good indicator, and soft-start features are included, only a few components are needed to complete the power supply design.
Pickering, the reed relay company which has pioneered miniaturisation and high performance for over 50 years, has signed a distribution deal with Tesco, the specialist distributor of passive, electromechanical and interconnect components based in Sunnyvale, CA.

The agreement means that Pickering’s large range of reed relays for A.T.E. switching and semiconductor test is now available and supported by the distributor across North America.

Included in the inventory of Pickering’s reed relays that are held by Tesco for immediate shipment are the 4mm2TM product family which feature industry’s smallest footprint - 4mm x 4mm.

Within the family, Series 120 devices have a switching rating of up to 1A at 20W and a height of 15.5mm, Series 122 relays measure 12.5mm in height and are rated with a switching current of 0.5A at 10W, and Series 124 products which feature industry’s lowest profile - 9.5mm - and a rating of 0.5A at 5W.

Pickering’s range of high voltage reed relays will also be offered from stock.

Nicomatic, a leading manufacturer of high-performance interconnect solutions, is launching Optimus, an EN4165-compliant, modular, rectangular I/O connector series. This low-profile interconnect solution is user-configurable and is applicable either to provide an equipment interface connection to a harness or as a robust rack & panel solution.

Conforming to specifications set out in EN4165, Optimus connectors are highly versatile. Modular construction enables designers to specify the layout they need. Connectors can be configured with size 22 signal contacts rated at 5A or size 8 power contacts rated for 60A. 90° PCB mount versions are also available. Devices are waterproof and offer EMI protection.

The new Optimus EN6145 connectors can withstand 500 mating and de-mating cycles as per EN2591-406. Devices also meet the shock and vibration requirements of EN2591-402/403 and have an operating temperature range of -55 to +175°C.

The connectors provide excellent protection against EMI and withstand 10 times lightning strikes of 10KA, 1600V.

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Automotive-grade ATPG

Siemens IC test for Zero DPPM

The Tessent test software brings advanced automation to the challenges of zero-defect ICs for automotive electronics.

The Tessent TestKompress with Automotive-grade ATPG software tool addresses the need for very high-quality ICs for automotive electronics by targeting defects within cells, at the transistor level. Traditional test methods are designed to capture defects in the interconnect between cells, and therefore miss a large, and growing, number of defects that occur in today’s complex transistors. Capturing these otherwise undetectable defects helps the makers of digital ICs meet the ISO 26262 goal of zero defective parts per billion (DPPB).

The Tessent TestKompress with Automotive-grade ATPG contains a suite of fault models and test pattern generation applications that can be used separately or together. The software is the result of decades of research in cell-aware, layout-aware, and defect-oriented test and modeling. These technologies were developed in collaboration with foundries, fabless companies, and integrated device manufacturers (IDMs). Tessent TestKompress with Automotive-grade ATPG has been validated on millions of test devices representing mature planar process nodes, as well as state-of-the-art FinFET processes.

With Tessent TestKompress Automotive-grade ATPG, users can target not only the cell-based faults, but can also start to introduce the same layout-based technology to address critical area-based interconnect and cell-neighborhood faults. Enabling structural test to reach DPPM levels that would otherwise only be possible by combining ATPG patterns with extremely expensive functional or system-level tests.

Mentor’s fault model extraction makes TestKompress cell-aware stand out from the crowd.

The fault extraction uses layout-annotated Spice representation of the cells to identify the location of possible transistor, bridge, open, and port defects. The extraction process automatically ranks bridges and opens on critical area, allowing ATPG to focus on the most important defect locations.

As the automotive electronics industry creates larger and more complex chips at the most advanced process nodes, they can rely on the Tessent family of products from Siemens to help them meet their required IC quality. To learn more, download the white paper: https://go.mentor.com/55fOr the product website: https://www.mentor.com/tessent
Communications networks are constantly evolving, migrating to increasingly higher speeds that raise the bar in terms of clocking and timing requirements.

The demand for more network bandwidth is driving the need for tighter timing synchronisation in addition to lower jitter, lower phase noise solutions.

Just as challenging, timing components must be affordable and compact, with designers looking for greater integration and fewer external components.

Two emerging applications that are pushing advancements in timing technology are AIoT (the combination of artificial intelligence and the Internet of Things) and 5G mobile networks.

**Advanced timing solutions**

AIoT technology can address the need for real-time processing of data from IoT sensors, especially when low latency is required. To meet this need, AIoT shifts data processing away from centralised data centres to new computing platforms at the edge of the network.

Edge computing requires a new class of low-latency IoT routers, servers, storage platforms, and specialised machine-to-machine (M2M) workload accelerators.

These applications require frequency-flexible clock generators, programmable oscillators and low skew/jitter clock buffers to provide clock synthesis and distribution.

In industrial IoT applications, data is increasingly being generated by sensors and machine vision systems and distributed across Ethernet networks.

Similarly, autonomous driving significantly increases the use of sensor networks and real-time data processing. Collectively, these applications require higher bandwidth and more data processing, increasing the need for high performance timing solutions.

**5G requires tighter synchronisation**

New 5G services are starting to roll out around the world, enabling faster, higher bandwidth mobile connections for more users. 5G will also enable better coordination between cell towers, helping to improve call quality and minimise dropped calls.

These new 5G services require higher performance, lower latency radio access networks (RAN). In terms of timing, 5G RAN requires tighter synchronization between the cell or base station towers, driving a growing need for more advanced timing solutions.

5G technology holds great promise for smart home and industrial IoT applications, which will connect far more devices to the Internet than at present. As a result, the amount of data that will be carried over 5G networks will grow rapidly in the coming years.

Much of this data will be stored in the cloud, requiring higher bandwidth connectivity across telecom networks.
to centralised data centres.

**Considerations when choosing a clocking solution**

To meet the demands of AIoT and 5G applications, system engineers must consider multiple factors when choosing clock ICs or designing a clock tree:

- **Performance** of the reference clock remains a top priority since it directly impacts the quality of a communications link. It’s a good idea to choose a clocking solution that provides significant jitter or phase noise margin in comparison to system requirements to ensure the quality of the wired / wireless transmission.

- **Cross-talk** is another issue to consider, since multiple copies of non-integer-related frequencies are often needed to provide the necessary reference clocking for an entire system. The simplest approach is to use multiple crystal oscillators, but a more integrated solution may be preferable to reduce BOM cost and complexity. In these situations, clocking solutions must be carefully selected to ensure cross-talk and interference are minimized. Cross-talk is configuration-dependent, so every new mix of frequencies can create new challenges.

- When **multiple clock signals** are required, the optimal level of integration that should be achieved is an important consideration. For simpler applications, designers may opt to use one or two basic crystal oscillators, but more complex applications require more clocks and more unique frequencies.

An integrated clock generator solution is typically smaller, cheaper and simpler to design with – but multiple, local clock sources may be better where it is difficult to route clock signals over long traces due to PCB design constraints and signal integrity concerns.

Each application may require a **specific set of frequencies**, which can make it difficult to find appropriate clocks. The best approach may be a customized timing solution.

**Broad range of timing solutions**

When assessing timing requirements for a complex AIoT or 5G application, it’s important to look for a vendor with a broad portfolio of clocking solutions and deep expertise in high-performance timing technology for high-speed networks and data centres.

For example, Silicon Labs offers best-in-class clock tree integration and jitter performance across its portfolio, enabling single-IC solutions for both high-volume, cost-sensitive designs as well as higher performance, more demanding applications.

For some applications, solutions with no external timing reference may be best for space-constrained designs. Over the past year, Silicon Labs has introduced a broad portfolio of clock generators and jitter attenuating clocks that eliminate the need for an external quartz crystal reference, simplifying PCB layout while improving overall system reliability. These devices are particularly well-suited for space-constrained applications that can’t afford the larger footprint required by more discrete solutions.

For the industrial IoT, Silicon Labs offers a broad array of cost-effective crystal oscillators and clock generators. For autonomous driving applications, Silicon Labs is developing new automotive-qualified timing solutions that will dramatically simplify clock synthesis and distribution while also increasing system-level reliability.

Always look for a vendor who is committed to providing state-of-the-art timing solutions that not only look to simplify clock synthesis and timing synchronisation in AIoT and 5G applications but that can provide best-in-class jitter and phase noise performance and clocking integration, that will enable you to adopt highly optimised, single-chip solutions that help accelerate the market adoption of AIoT and 5G.
A thermal runaway is an increasing threat to electronic devices where more and more power is packed in ever smaller spaces; it is a threat that is poorly dealt with using traditional means. SMD thermal fuses offer a solution that can be reflow-soldered at 260°C and still open at 210°C.

What is meant by a thermal runaway or the thermal damage of power semiconductors? A thermal runaway refers to the overheating of a technical apparatus due to a self-reinforcing process that generates heat. This damage usually causes the destruction of the apparatus and often leads to a fire or explosion.

The causes of a thermal runaway are varied and often random in nature. However, the ever-higher power density in electronic wiring and the trend towards miniaturisation are of particular importance. More and more functions are packed in compact modules, which then also have a correspondingly high power consumption. Even slightly excessive currents in power electronics with only a little power loss lead to elevated temperatures of approximately 200°C. The possible consequences are damage or disconnection of surrounding components, damage to the printed circuit board structure or in the worst case, the triggering of a fire.

With a power semiconductor (e.g. MOSFET) the drain-source transmission resistance increases with rising temperatures when connected, which results in an increasing loss of power in the barrier layer. If the elements are not sufficiently cooled - the high power density permits cooling - the power loss output in the form of heat can no longer be sufficiently dissipated, which also increases the transmission resistance. This process escalates and ultimately leads to destruction of the component.

How to protect against a short circuit? The cooling of a system must dissipate at least as much energy as it is supplied with. The overcurrent during a thermal runaway is too low to cause a conventional fuse to trip. Thermal circuit breakers or PTCs would in principle be used, but the products available for the assembly of an SMD printed circuit board are too complicated or completely unsuitable.

The SCHURTER Solution
SCHURTER has developed and manufactured the RTS Reflow Thermal Switch. The RTS can be reflow soldered @ 260°C after which it is mechanically activated and can still effectively trip at 210°C. Now available with an integrated current measuring sensor (Shunt) enabling precise current measurement. The RTS is optimised for standard SMD processes like pick and place other features include:

- High operating current up to 130 A
- High rated voltage 60 VDC competition is limited to 16 VDC
- Low resistance: 120µOhm
- Very high Breaking Capacity 400A

- https://uk.schurter.com/content/download/2357131/40537784/file/ApplicationNote_TermalRunaway_EN.pdf

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Leveraging your digital twin

Look at the mirror and foresee the future of telecommunications, by Claus Nielsen, Vice President of Marketing at Neural Technologies

The adoption of 5G will unleash the full potential of augmented and virtual reality, Smart Cities and the Internet of Things (IoT); presenting opportunities for Communications Service Providers (CSPs) to strengthen current revenue sources or create entirely new revenue streams. Consumers continue to display an insatiable appetite for data and with the consumption of data hungry applications securing a place in consumers’ daily lives, this is set to continue exponentially into the future.

Communications Service Providers currently face ever-increasing challenges of leveraging 5G networks and offering customers new types of services. To overcome this challenge, new digital technologies are required to automate complex business processes to provide customers with the new personalised service they have come to expect in a fast-evolving, digital world.

By 2025 Communications Service Providers should already be leveraging 5G networks to offer new types of services to various customer segments. The challenges of this endeavour will lie in the ability to scale telco platforms, automate lifecycle management of network slices and incorporate predictive demand and maintenance - all while ensuring operational efficiency and a behind the scenes workforce to support the optimisation of the platform.

Using automation

To address these challenges, an Analytical Data Model (AD Model) and Machine Learning (ML) were used to develop the Digital Twins technology and tested as part of the TM Forum Digital Twins catalyst project.

The technology serves as a virtual representation of a real-world entity or system which acts as a mirror to provide a means to simulate, predict and forecast behaviour in the digital world. As part of the catalyst project, the Digital Twins technology was applied to various use cases such as a network, people, organisations and processes to determine their effectiveness in being applied to the telecoms industry in order to address the above 2025 challenges.

For the Digital Twins technology to be possible, a common data model is essential. All data needs to be classified and structured in the same way for the digital technology to perform. Digital Integration is the first step to making this possible.

One example of a Digital Twin is that of a customer. Such Digital Twin of a customer will be represented in a heatmap with icons helping to visualise aspects of their digital lifestyle, such as whether they spend a lot of time gaming, have high mobile usage and are physically inactive. This twin can then be used by the...
Communications Service Provider to tailor messages to that individual. For example, the Digital Twin may show that the customer has a low step count which could trigger a notification to the individual to be more active.

Using a Digital Twin, operators can also determine where there will be a significant increase in latency within the network and then share that information with the customer’s Digital Twin to find out what is going to be affected to determine the next best action.

The Digital Twin can also speed up product development cycles, save time and money and create new business models based on intelligent outcomes, allowing enterprises to personalise the customer experience and meet their precise demands. In return, this enables enterprises to grow and improve their customer base through targeted campaigns and provide tailored services and promotions. In turn, this generates greater customer loyalty and retention as well as customer spending through personalisation with timely bespoke offers.

Proven methods for the future
The TM Forum Digital Twins catalyst project proved that Digital Twins not only work for the manufacturing industry but for the telecommunications space as well. As part of the project, Neural Technologies successfully created a Customer Twin alongside the collaborative development of a Mobile Network Twin and an Enterprise IP Network Twin all originating from the core AI Data Model.

In addition, the catalyst project also demonstrated real-time communication between the twins. Using the proposed TM Forum Open Application Program Interfaces (APIs), Neural Technologies was able to share such simulated, forecasted and predicted outcomes so that each individual twin was able to recommend a more informed action, instead of a siloed view.

Ultimately through using Digital Twin technologies in the telecommunications industry, a more holistic view across the whole of the operator’s network will be achievable, making it possible to not only make more informed recommended actions but equally faster decisions. As a result, all such ‘what if’ scenarios could now be done in the virtual world without affecting the real world.

Next to the challenges the telecommunications industry will face with the ever-growing volumes of usage data, software vendors like Neural Technologies need to provide solutions which are able to exchange data with any kind of connected system. Information exchange between systems will be key and the usage of real time Application Program Interfaces will grow. Industry standards for these APIs, like those specified through the TM Forum Open APIs, will help to standardize the exchange of information which Neural Technologies fully support already today.

With more data becoming available through the Internet of Things and 5G in the future, operators need to prepare themselves to leverage this data. Data is every operator’s asset, using Artificial Intelligence and Machine Learning, these assets can be mobilised to enable Communications Service Providers to strengthen current revenue sources by creating entirely new revenue streams. Ready to help Communications Service Providers achieve these goals, Neural Technologies’ state-of-the-art digital transformation and analytical technologies can help CSPs to leverage this data and create new revenue streams.
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