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AUTOMOTIVE ELECTRONICS • DISPLAYS • COMMS TEST • INTERNET OF THINGS

PROCESSING THE MOBILE MARKET

With 5G and foldables hitting headlines, how are incoming technologies effecting mobile usage?

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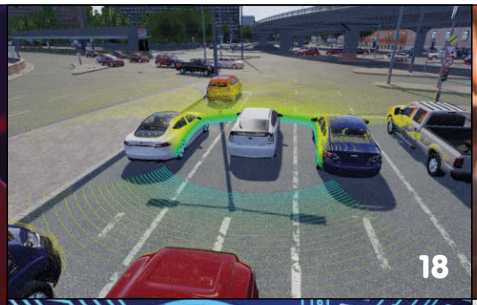

MISSION STATEMENT

'New Electronics keeps designers and managers abreast of the latest developments in the world's fastest moving industry'

Wake up and smell the coffee

WHEN IS UK PLC GOING TO WAKE UP TO THE VALUE OF AUTOMATION WHEN IT COMES TO RAISING PRODUCTIVITY AND IMPROVING JOB SATISFACTION?

A recent briefing by the British Automation and Robot Association (BARA) together and VDMA, Europe´s network organisation for mechanical engineering, highlighted how poor the UK's record has been in deploying and using robots.

In terms of industrial robots installed, the UK comes in at a lowly 22nd with just 91 units installed per 10,000 employees.

In Europe, five countries Germany, Sweden, Denmark, Belgium and Italy make the global top 10 and in countries like Singapore and South Korea the numbers installed are 831 and 774 per 10,000 employees, respectively.

The benefits of automation are well documented. It's more efficient when it comes to the use of resources, it significantly improves levels of productivity and enables much greater flexibility, and can provide people with more rewarding jobs - they no longer have to do dirty, dull and monotonous routine ones.

Worries about robots taking jobs seem to be overblown as research from Germany points to quite the opposite outcome, with increased levels of investment in technology accompanied by a jump in employment. In fact, the use of smart industrial robot systems has improved the chances of higher quality work for employees.

In the UK businesses seem to have preferred to hoard cheap labour to throw at raising levels of production. The argument that the UK's manufacturing base is dominated by SMEs, which means that there just isn't the demand for robots when compared to countries where much larger manufacturing businesses operate, no longer holds true either with the development of cheaper robots and cobots.

How ever you look at it, the UK is performing badly and if we want to be economically successful this is going to have to change as we enter a post-Brexit world.

Immigration plans, recently unveiled by the government, want the UK to move away from relying on "cheap labour" from Europe and rather invest in training staff and developing automation technology.

Research shows that the working population in the UK want better education and training for working with robots and that it should be a top priority for policy makers.

We can but hope, but with the government reverting to form and failing to deliver on its own industrial strategy, the onus on raising investment in automation is likely to fall on businesses themselves.

This raises the question as to why businesses have been failing to invest enough and engage more with automation.

Is it to do with a culture that fails to look at the longer-term, or that has relied too heavily on cheap labour for too long, or one that is simply risk-averse when it comes to automation?

Is it because we have a fetish for sweating our assets and keeping machines running well past their sell-by dates, rather than regularly investing in the latest technologies and systems - I doubt many German or Japanese companies celebrate the fact that they are still using machinery first installed 30, 40 or 50 years ago.

We've cut ourselves off from our biggest trading market and we are now competing directly with the likes of China, Singapore, South Korea and the US.

After Brexit, businesses are going to have to use their workforce far more effectively and, as a matter of urgency, embrace automation if they are to survive, let alone remain competitive.

Neil Tyler, Editor (neil.tyler@markallengroup.com)

> "How ever we look at it, the UK is performing badly and if we want to be economically successful this is going to have to change as we enter a post-Brexit world"

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Long term collaboration

MARVELL AND SAMSUNG LOOK TO DRIVE INNOVATION IN A NEW GENERATION OF 5G INFRASTRUCTURE PRODUCTS. **NEIL TYLER** REPORTS

Marvell and Samsung Electronics have announced that the companies are extending their collaboration to encompass infrastructure innovations across additional segments of the Radio Access Network (RAN). Marvell and Samsung have worked closely to deliver multiple generations of baseband and transport processing solutions for base stations based on Marvell's OCTEON and OCTEON Fusion processors.

In addition, the companies are collaborating on innovative radio unit architectures that are being designed to meet the dramatic increase in compute power required for the complex beamforming algorithms inherent to massive MIMO deployments.

Building on the OCTEON Fusion platform and integrating Samsung's IP will provide a differentiated offering, while speeding time-to-market with optimised solutions.

Network operators are facing the challenge of rolling out cost-effective 5G network infrastructure, while addressing the complexities of higher spectrum frequencies, massive MIMO antenna arrays and super low latencies. The collaboration between Marvell and Samsung will look to address these issues by developing highly integrated solutions with improved levels of programmability and performance.

Based on the OCTEON Fusion platform, these solutions are also immediately enabled by the broad software ecosystem it provides.

"Samsung is committed to helping mobile operators meet their performance targets," said Jaeho Jeon, executive vice president and head of R&D, Networks Business at Samsung Electronics, while Raghib Hussain, chief strategy officer and executive vice president of the Networking and Processors Group at Marvell added, "It is our goal to ensure that infrastructure equipment suppliers can allow network operators to thrive in the fast-paced world of 5G."

Plextek Group Sells Plextek RFI to CML

Plextek Group has announced the sale of one of its spin-outs, the boutique microwave chip design business Plextek RFI to CML Microsystems for an undisclosed sum.

Plextek RFI specialises in designs of RF, microwave and mmWave ICs and modules. To date the team has completed in excess of 100 IC designs, operating at radio frequencies up to 100GHz and is a third-party approved design house for semiconductor companies globally.

Design experience includes front end ICs for mm-wave 5G, broadband Monolithic Microwave ICs (MMICs), receiver, transmitter and power amplifier (PA) ICs for microwave links and GaN PAs.

The designers, IP, order book and customer relationships are all part of the deal, which represents the first outright sale of one of the Plextek Group companies which include: Plextek Services, Blighter Surveillance Systems, Redtail Telematics and Telensa.

"PRFI enhances our strategy for expansion within communications markets and expands our existing skills, services and consulting income stream for CML" explained Chris Gurry, CML's Group Managing Director.

STMicroelectronics to acquire GaN innovator

STMicroelectronics has signed an agreement to acquire a majority stake in French Gallium Nitride (GaN) innovator Exagan.

The company specialises in epitaxy, product development and application know-how and will, according to ST, help to broaden and accelerate the company's power GaN roadmap.

Terms of the transaction were not disclosed but it does provide for the acquisition by ST of the remaining minority stake in Exagan 24 months after the closing of the acquisition of the majority stake. The transaction is funded with available cash.

"ST has built strong momentum in silicon carbide and is now expanding in another very promising compound material, gallium nitride, to drive adoption of the power products based on GaN by customers across the automotive, industrial and consumer markets" said Jean-Marc Chery, President and CEO of STMicroelectronics.

He continued: "The acquisition of a majority stake in Exagan is another step forward in strengthening our global technology leadership in power semiconductors and our long-term GaN roadmap, ecosystem and business."

Percepio's Tracealyzer 4.4 supports Embedded Linux

Percepio, a specialist in visual trace diagnostics for embedded systems and IoT, introduced support for embedded Linux systems with the launch of Tracealyzer v4.4 at Embedded World.

This latest version of Tracealyzer includes visualization and analysis capabilities intended for embedded Linux application developers.

Tracealyzer transforms low-level trace data into a rich set of overviews enabling top-down exploratory analysis, making it easier to spot anomalies and drill down to see the details.

Tracealyzer for Linux leverages the widely supported LTTng tracing framework, and has been verified with Wind River Linux LTS 2019.

"Wind River has teamed with partners such as Percepio AB to ensure that there is both an open source and a commercial ecosystem of tools that address the needs of Wind River Linux developers," said Wind River in a statement. "The Percepio Tracealyzer trace visualization tool provides a large number of high-level views to make it easier to spot anomalies in program execution and to trace them to the root cause without requiring a great deal of Linux kernel expertise."

Tracealyzer v4.4 combines the latest generation Tracealyzer with significant improvements for embedded Linux including a rich set of high-level overviews for top-down exploratory analysis, user-defined Advanced Analysis as well as leveraging CTF, the Common Trace Format, using the LTTng tracing framework.

According to Percepio CEO Dr. Johan Kraft, "There is tremendous potential to improve embedded software development via better insight into the runtime system in complex software systems based on Linux. Proper tools for visual trace diagnostics are key as they allow developers to make sense of large software traces, identify bugs and verify solutions."

Multi-touch screen display

TANVAS UNVEILS PROGRAMMABLE EFFECTS AND TEXTURES FOR AUTOMOTIVE DISPLAYS. **NEIL TYLER** REPORTS

Tanvas, a specialist in multi-touch haptic technology, has unveiled a piezo-free, non-vibrating automotive multi-touchscreen display that will enable manufacturers to produce custom, programmable textures and haptic effects on a screen's smooth glass surface.

The 15" display, developed in partnership with Innolux, implements TanvasTouch technology to produce a wide variety of software-defined textures and haptic effects. Streamlined surfaces are increasingly replacing physical knobs and dials inside the cabin, and this technology assists the driver to find and adjust controls while keeping their eyes on the road.

The solid-state TanvasTouch technology, which uses an electric field to modulate friction locally where the user's fingers move across a surface, is a replacement for traditional vibrotactile haptics in automotive applications.

Unlike electro-mechanical haptics, solid-state, the company'd haptic technology can be implemented in any display format, including large and curved displays and can be deployed on surfaces of any shape.

Suitable substrates include glass, plastic, metal, ceramics, and natural surfaces and the technology provides freedom for the car manufacturer to create a uniform or harmonious touch experience across multiple surfaces – not only the display screen, but also the steering wheel, exterior door handle and even upholstery.

KIOXIA debuts UFS Ver.3.1 devices

KIOXIA Europe (formerly Toshiba Memory Europe) has started to sample Universal Flash Storage (UFS) Ver. 3.1 embedded flash memory devices. Intended for mobile applications including 5G networks requiring high-performance with low power consumption, the line-up utilises KIOXIA's BiCS FLASH 3D flash memory and is supported in four capacities: 128GB, 256GB, 512GB, and 1TB.

These devices integrate BiCS FLASH 3D flash memory and a controller in a JEDEC-standard 11.5mm x 13.0mm package. The controller performs error correction, wear levelling, logical-to-physical address translation, and bad-block management for simplified system development.

According to the company, these latest offerings will enable next-gen mobile devices to take full advantage of the connectivity benefits of 5G, leading to faster download and reduced lag time.

All four devices include: WriteBooster capabilities, significantly boosting faster write speeds, sequential Read performance, Host Performance Booster (HPB) Ver. 1.0, which improves random read performance by utilising the host side memory and a UFS-DeepSleep Power Mode, which achieves a power consumption reduction in sleep mode compared to the existing UFS-Sleep Power Mode. A Performance Throttling Event Notification can also be deployed if the internal temperature reaches its upper limit, avoiding overheating and damage to the internal device circuits.

mVision accelerates embedded vision development

Lattice Semiconductor has announced the introduction of the Lattice mVision solutions stack.

The stack includes modular hardware development boards, design software, an embedded vision IP portfolio, and reference designs and demos needed to implement sensor bridging, sensor aggregation, and image processing applications.

The mVision solutions stack is intended to accelerate and simplify the implementation of embedded vision systems such as machine vision, ADAS, drones and AR/VR for the industrial, automotive, consumer, smart home, and medical markets.

"Lattice is committed to delivering complete solutions stacks, that accelerate the adoption of the disruptive technologies driving growth across multiple end markets," said Deepak Boppana, Sr. Director of Segment and Solutions Marketing, Lattice Semiconductor. "With our Lattice mVision solutions stack, we are looking to bring the ease-of-use benefits of our solutions stacks, as well as the performance, reliability, and power savings made possible by our new Nexus FPGA development platform, to the embedded vision market."

Key features of the mVision solutions stack include: Video Interface Platform (VIP), a comprehensive IP library, FPGA Design Tools - the stack supports both of the company's easy-to-use FPGA design tools - and a range of complete reference designs for common embedded vision applications as well as Custom Design Services.

STT-MRAM for IIoT Applications

At Embedded World, Everspin Technologies announced the development of STT-MRAM specifically for Industrial and IoT applications. The company is developing a new STT product family to dress the needs of broad industrial applications, providing improved data persistence, 8Mb to 256Mb densities, a -40 to 85°C operating temperature range and SRAM-like performance.

With the increasing bandwidth, features, code and data storage requirements for industrial applications driven by 5G, the need for higher densities is expected to accelerate.

MRAM is often used as a universal memory in these applications, being fast enough to execute code as well as provide persistent storage for all data captured.

The new Industrial/IoT STT-MRAM will deliver densities of 8Mb to 256Mb, complementing and extending the current Toggle MRAM Serial interface products of 128Kb to 4Mb. To complete the portfolio, Everspin provides Toggle Parallel interface devices up to 32Mb and a 1Gb STT-MRAM with a DDR4 interface for the data centre market.

Maxim announces two LiDAR ICs

Maxim launched two LiDAR ICs at Embedded World, the Max400026 comparator and Max40660/Max40661 transimpedance amplifiers.

According to Maxim, these ICs represent a twofold increase of bandwidth and, at 128, an additional 32 channels over the nearest competitor in the same size module. The Max40026 is provided in a TDFN package size of 4mm^2 while the 40660/1 come in a 9mm^2 TDFN package.

Maxim says the devices enable increases of 10mph for autonomous driving systems at highway speeds.

These improvements are designed to provide designers with higher image quality, allowing the sensors to more accurately measure the environment.

The Max40660 has a bandwidth of 490MHz with 0.5pF input capacitance and 25kΩ transimpedance and a 2.1pA/√Hz input-referred noise density. The Max40661 has a typical bandwidth of 160MHz with 10pF input capacitance. The Max40026 additionally features a 10ps propagation delay dispersion for the detection of fixed and moving objects.

These ICs meet the automotive-grade AEC-Q100 qualification, enhanced electrostatic discharge (ESD) performance and failure modes, effects and diagnostic analysis (FMEDA) to support ISO 26262 certification at the system level.

LiDAR sensors are an essential part of ADAS systems, using pulses to measure the range and distance between the vehicle and other objects in the environment.

Wind River Labs unveiled

Wind River announced the introduction of Wind River Labs, a new developer-focused site where technologists can gain access to software projects, proof-of-concepts, open source integrations, experimental software, and new technologies.

The site includes the first-ever freely available VxWorks real-time operating system (RTOS) software developer kit (SDK) for the developer community.

Wind River Labs is an environment that has been developed to support developers, both Wind River customers and non-customers, looking to innovate at the edge, enabling capabilities such as machine learning and computer vision.

This includes interacting with the software engineers who created the projects, other software engineers tackling similar challenges, and Wind River ecosystem members exploring new markets and forward-looking designs.

The available VxWorks SDK includes an open source board support package for Raspberry Pi and UP Squared hardware. Developers can now download the latest version of VxWorks, along with projects such as ROS (Robot Operating System) 2, and immediately start prototyping and designing applications on the company's industry-leading operating systems.

"With the amount of software content proliferating, and autonomous and intelligent systems significantly growing in relevance, driving collaborative innovation is more important than ever," said Gareth Noyes, chief strategy officer at Wind River. "Wind River Labs gives developers early access to cutting edge software projects, and allows the sharing of ideas through working code, examples, and recipes for technologies and community projects."

Jiva Materials looks to deliver fully recyclable PCBs

Sustainability start-up, Jiva Materials, has completed a £750k seed funding round to help fund the development and commercialisation of Soluboard - a material designed to make printed circuit boards fully recyclable.

Around 18 billion square metres of PCBs are manufactured every year and with the rising value of the precious metals within PCBs and an increasing global awareness of environmental issues, more efficient recycling is fast becoming a necessity.

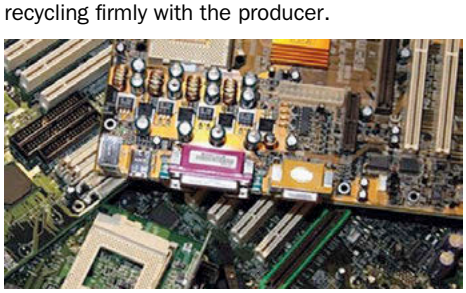
Jiva Materials' patented, fully recyclable PCB substrate, is intended to rival the industry standard, FR-4.

FR-4 is made from epoxy resin and fibreglass which means that the only method of processing waste PCBs involves shredding and incineration to extract the precious metals within – this process is both inefficient and releases Persistent Organic Pollutants (POPs) into the environment.

The organic structure of Soluboard means the non-toxic ingredients begin to delaminate when immersed into hot water, allowing the natural plant-based fibres to be composted, the remaining solution to be disposed of using standard domestic waste water systems and the electronic components to be removed for re-processing.

On a global scale, an estimated 50 million tonnes of Waste Electrical and Electronic Equipment (WEEE) was produced in 2019. Small domestic scale electronic products make up the majority of the weight of this WEEE, with 8% of the weight of these products coming from PCBs.

EU domestic appliance and white goods manufacturers have confirmed a growing interest in Soluboard as tighter regulations are being placed on manufacturers of electronics to put the responsibility of recycling firmly with the producer.



A current map for improving circuit design

RESEARCHERS ARE ABLE TO MAP THE FLOW OF CURRENT IN COMPLEX GEOMETRIES. **NEIL TYLER** REPORTS

Researchers at KAUST have unveiled a method for mapping the flow of a current in devices with complex geometries, that could be used to optimise circuit design.

Senfu Zhang and Xixiang Zhang, working with colleagues from KAUST, China and the United States, have devised a method for visualizing the magnitude and direction of current flow through a magnetic thin film.

Several experimental methods had been developed to map current density in electronic materials, but these only do so indirectly, measuring stray fields rather than the currents themselves and can be expensive to implement.

Computer simulations offer a cheaper alternative; however, they tend to oversimplify actual devices, ignoring non-uniformities or cracks in the material.

The team have been able to directly map the non-uniform electrical current distribution in layered platinum, cobalt and tantalum using skyrmions. These "magnetic bubbles" can be imaged by a technique known as magneto-optical Kerr microscopy, which measures changes in the intensity and polarization of light reflected from a surface as a result of magnetic disturbances.

The skyrmions appear as round bubbles in the microscope images.

"We found that when we passed a current through the material, only the front end of the bubbles moved forward, forming narrow, parallel strip domains," explained Senfu Zhang. The researchers have been able to show that it is possible to extract the current flow from the growth direction of these patterns.

"This approach is not suitable for use in an actual devices because it requires the deposition of Pt/Co/Ta on the device, but it is useful in the design phase," explained Zhang. "Knowing the direction and magnitude of the electric current in each part of the device helps improve the design and performance."

Lux predicts energy storage market to be worth **$546bn by 2035**

The total energy storage market is expected to grow to $546 billion in annual revenue by 2035, according to a report released by Lux Research.

The report, 'The Global Energy Storage Market 2019', estimates that the three main drivers of energy storage – mobility applications, electronic devices, and stationary storage – will reach an annual combined deployment level of 3,046 GWh over the next 15 years, up from 164 GWh, at present.

"The energy storage industry is poised for a massive increase in annual revenue and deployment capacity as key innovative technologies, such as solid-state batteries and flow batteries, reach commercialisation," said analyst Chloe Holzinger, one of the report's lead authors.

"We continue to expect electric mobility applications to be the principal long-term driver of energy storage annual revenue and demand, with a total market share of 74% by annual revenue and 91% by annual deployed GWh by the year 2035."

Growth in revenue and deployment for the energy storage market over the next three years will be markedly different from the overall 2035 projections, with plug-in light-duty vehicles remaining the largest market with a predicted $24 billion increase in revenue by the end of 2022.

Residential storage has a CAGR of 76% and $8 billion revenue increase over the next three years, followed by personal mobility with a CAGR of $49% and $4.6 billion revenue increase.

Mobility applications remain the long-term growth and demand driver for energy storage through 2035, with personal mobility devices expected to increase to $43.7 billion from their current $2 billion in revenue.

IT'S ALL **CHANGE**

From the network to usage, innovations in the mobile sphere are unfolding at an accelerated rate. By **Elliot Mulley-Goodbarne**

Amongst a bombardment of advertising from your favourite Californian conglomerate, every September a debate will break out about the cost of mobile devices.

After Apple burst through the four-figure barrier in 2017 we have seen prices for all devices, from iOS and Android manufacturers, grow to the point where the latest S20 is nudging £1,500.

While that for a phone might seem excessive it does include a biometric authentication technology that Fort Knox would be proud of, a camera with the ability to record in 8K and the capacity to reach internet connection speeds the envy of domestic lines. These mobile phones have the capability to carry out tasks we would have needed three different devices to deliver 10 years ago.

One such function was realised at Samsung's launch of its flagship 'Galaxy S' range, earlier this year. At the presentation, it managed to use its latest device's capability to record video in 8K resolution to stream the show live from San Francisco.

Camera quality has long been a differentiator when it comes to mobile sales, with a growing number of advertising boards featuring the tag line 'Shot on an iPhone'. Such differentiation is being played out before our eyes with Apple, Samsung, Google and Huawei using a layer of artificial intelligence on top of physical camera sensors.

Speaking at a press event for the S20 series, Samsung mobile head of product management, Paul Scott said, "One of the challenges with the design of a smartphone and the camera is how do you get a zoom lens into a smartphone? With the S20 Ultra we have been able to deliver a super slim design, but still have up to 100 times zoom. It's an incredible R&D achievement."

The camera module on the latest device features a 12MP ultra-wide, 108MP wide angle and 48MP telephoto sensor set up with the ability to achieve a 10 times optical zoom. That zoom is achieved using periscopic technology that allows light through the 48MP slot to be beamed back to the sensor. That hardware technology is combined with software that combines multiple pixels together in a process called 'binning' once the zoom exceeds 4x.

"People are trying to get the best shot, whether it's a footballer or it's a person on stage, and what they always fail on is trying to zoom in and get a good quality shot.

"What you can now do is not only

9parusnikov/stock.adobe.com

take great photos in low light, but also achieve zoom levels up to 100 times so a user will be able to get the best photo possible."

The importance of smartphone photography is backed up by HMD Global head of design Raun Forsyth. HMD Global hold the brand licence for Nokia mobile phones and have hit the headlines at Mobile World Congress for its retro handsets but also for the Nokia 9 device which has a five sensor camera set up.

Alongside having the unexpected ability to send trypophobics into a frenzy, the sensors were needed to capture a high dynamic range of brightness and contrast and sense different depths as HMD Global looked to address the needs of professional photographers.

"When we launched the Nokia 9 PureView, featuring the world's first five camera array with ZEISS Optics, we had photography enthusiasts in mind. They demand the very latest technology to capture their images" said Forsyth.

ARM vice president and general manager of Client Line of business Paul Williamson added that photography is one of the biggest drains on compute performance in mobile devices.

"Improvements in camera systems are driving requirements across the whole system, from the pre-processing directly on the sensor, to post-processing on the main SoC where CPUs and GPUs are heavily used for DSLR-class blurring of pictures to mimic larger optical scopes and Bokeh effect.

"The need for processing more data pushes for higher single thread performance on the CPU, while camera enhancements are pushing ML capabilities across the whole platform, all for the same power budgets and full day or multi-day battery life."

Growing 5G impact

It's impossible to talk about mobile technology without mentioning 5G. The latest networks, launched by all four operators, are set to trigger a fourth industrial revolution in manufacturing according to certain analysts, but the immediate focus is on selling phones.

In short, 5G is touted to be the bridge between almost exclusive cellular connectivity for mobile devices, to having the ability to connect all electrical items to a cellular network rather than in house fixed or wireless internet access.

Focus is still very much on the mobile, with downloads speeds, in theory, able to deliver gigabits of data per second speeds - downloading movies and streaming the latest albums is just the start.

Features like edge computing and low latency data request and delivery open up new capabilities including streaming in virtual reality and gaming.

"When you look at the way data is generated and processed, the demands at the edge of the network are increasing significantly more than even in the data centre" suggests David Fraser, Intel technical sales manager for communication service providers.

"For something like gaming, being able to offer that low latency capability, pushing the content to the network is important so the gamers get that responsiveness and continue to have a good experience without having to process everything on the device.

"It's crucial that apps are able to support all different types of form factors, to provide a seamless user experience across the different screens"
Paul Williamson

"We're seeing [gaming] as one of the key use cases within that 5G space. Especially with the virtual and augmented reality experiences, the latency element becomes even more critical to provide a good experience otherwise the user will feel nauseated."

On the Network side ZTE president of global sales Xiao Ming said, "there are a lot of the things need to get improved" before those 5G uses can take off.

"There is a whole ecosystem and we, as a key driver, are talking to most of the hardware manufacturers to put effort in; but it is like the chicken and the egg.

"If we don't push ahead with a 5G ready network, then there will be no possibility for those hardware manufacturers or software businesses to further develop their solutions unless they have that incentive.

"For example, if you want to make VR lenses really popular for people to use, the current shapes won't fly. It's too heavy, it's not easy to wear, the mobility is an issue and it's really inconsistent with human habits. We'll need to have more powerful CPUs, GPUs, cameras and VR and AR processing capabilities."

One of those chickens (or eggs depending on your point of view) is Samsung, which embraced the gaming industry with its Note 9 device launched in summer 2018. "Just from a usage point, one that really stands out for 5G has been gaming," said Scott. "They get mega competitive in the gaming world and 5G will allow them to connect quickly."

"When using a device, gamers need the best refresh rate and want the most reactive screen possible. Now we have 120Hz refresh rates so it's going to look really clear and really smooth."

Below: Periscopic technology, like this example from Oppo, is helping vendors introduce optical zooms on smartphones

Cutting Edge

According to Williamson and Fraser, when it comes to 5G content, we have barely scratched the surface of what will be possible of a mobile device.

While live gaming appears set to be the first use case, Fraser has called for a re-imagination in the way that content is created.

"I think people who are designing applications or games need to look holistically at what compute resource they have on the device, the edge, and back in the data centre, and then design something that spans those three domains.

"The other critical factor is being able to write software that can utilise compute at the edge, the data centre and on the device. It's becoming more challenging with heterogeneous architectures."

"5G will open up new use case possibilities and opportunities for developers to take full advantage of a heterogenous platform, to reach maximum performance without draining the battery" said Williamson.

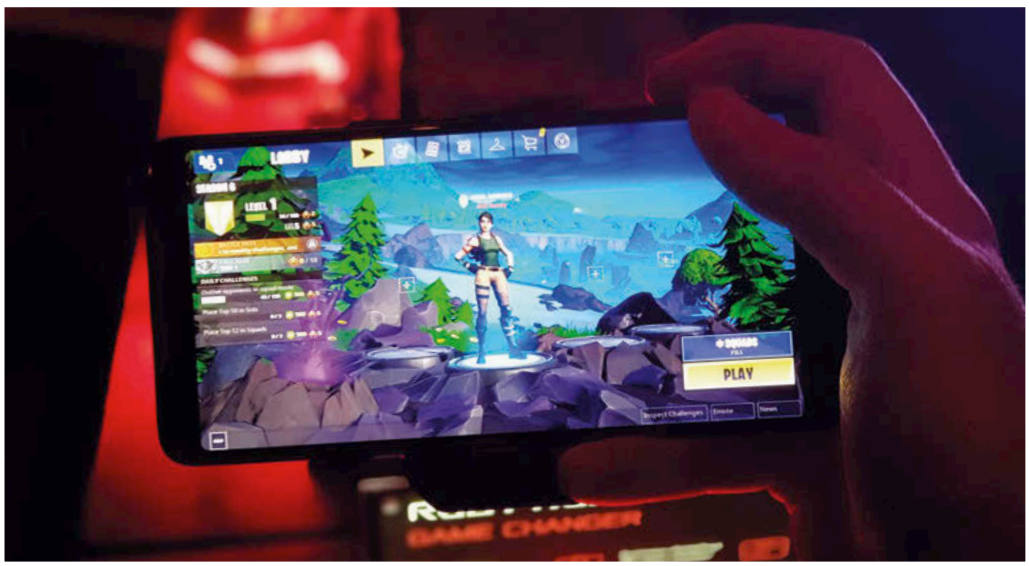
"The availability of 5G and the massive amounts of increased data funnelled through it will push every aspect of the end device, as well as the need for more efficient processing in the data centre.

"5G will unlock a new wave of highly immersive digital experiences which will demand more compute performance.

"There's a huge opportunity for developers to take advantage of 5G infrastructure to design and deploy these new use cases for edge devices with a drastic reduction in latency and instantaneous responsiveness."

Unravelling foldables

Another headline grabber has been the foldable device, a number of which were announced last year. Huawei, Samsung and Motorola got in on the act in 2019, although Samsung was the only one to make its Galaxy Fold device available to consumers.



High quality, live mobile gaming is expected to grow in the 5G era

2020 has seen two foldable devices hit the consumer market already with a new form factor. Both Samsung and Motorola decided to go with a horizontal fold with the Z Flip and Razr devices respectively, compared to the vertical fold seen in the Galaxy Fold.

Scott said that, when it comes to the design of devices, Samsung's priority is "pushing boundaries" whilst also giving practical reasons why someone would go for a folding display. He also said that Samsung has not settled on a specific form factor, adding, "We are absolutely looking at different options.

"The capabilities of Samsung and the investments that we've made in screen technology and design are huge. The screen is normally one of the top three influencers in any smartphone decision, along with the camera and battery.

"Consumers are using their devices more than ever before, but they need a screen that is big enough to watch all forms of content and a design that allows our consumers to do that."

According to Williamson, the chipset manufacturers are ready for the foldable revolution, adding "Foldable devices bring more screens and changing capabilities which require more processing power to build the smarter systems.

" The screen is normally one of the top three influencers in any smartphone decision, along with the camera and battery"
Paul Scott

"As mobile OEMs are building out these designs, the biggest challenge comes from a software perspective as it's crucial that apps are able to support all different types of form factors, to provide a seamless user experience across the different screens.

"Mobile processors are powering devices from feature phones, smartphones, and tablets to large-screen devices such as PCs and DTVs. The load on the system is different, but the capability of the processor is the same and we have seen this proven by the different designs hitting the market from Android, Windows, and Chrome, covering a range of UX from immersive mobile gaming to connected PCs for productivity on the go.

"Multi-tasking and multi-processing are already heavily used today in non-foldable devices. Gaming is a good example where there is a need for efficient multi-core performance on CPUs or GPUs. Foldable designs will increase the need for multi-core performance even further and these new device form factors will bring additional need for peak performance, but also more efficient designs," Williamson concluded.

Extreme machines

Neil Tyler talks to Paul Hart, CTO, Curtiss Wright Controls Avionics and Electronics about the challenges confronting suppliers to the military

Few companies have the historical pedigree of Curtiss Wright, formed in 1929 out of the merger of companies founded by Glen Curtiss, a leading innovator in naval aviation, and the Wright Brothers.

Over the past 90 years the company has changed immeasurably and today can claim leadership in advanced technologies for high performance platforms and critical applications, in sectors including industrial, power and defence.

When it comes defence the company supports a wide range of different programmes across naval, aerospace and ground defence markets linked by a host of sophisticated embedded computing products and electronics – it's a market that, like most others, is facing massive challenges and, according to Paul Hart, the company's Chief Technology Officer for Controls Avionics and Electronics, "The pace of change has been truly astounding and the challenges are certainly significant. Today's supply chain has been set up to address the needs of consumer electronics and not the military. It's not been designed to address the problem of obsolescence, which is a critical issue for the military.

"It's the overarching shadow that looms across almost everything we do," he concedes. "We need to be able to mitigate the component-level risk of obsolescence and that can only be done by designing with open architectures that will enable easier part replacement.

"It requires better and more proactive planning when it comes to inserting new technology into a programme that, in many cases, will have a long active life."

All of this requires extensive support for programmes and sourcing off-the-shelf (COTS) parts.

"Curtiss Wright looks to work with open architectures. We have to ensure that programmes are able to run continuously, and should a new component be required, a processor for example, that it can be run in a mode that will emulate a previous generation," Hart explains.

Open architectures are critical because long service military equipment may need to be deployed in a manner that's completely at odds with its original specification.

"The nature of warfare and the threats countries face continue to evolve, so the ability to upgrade equipment and adapt it to address new threats is critical.

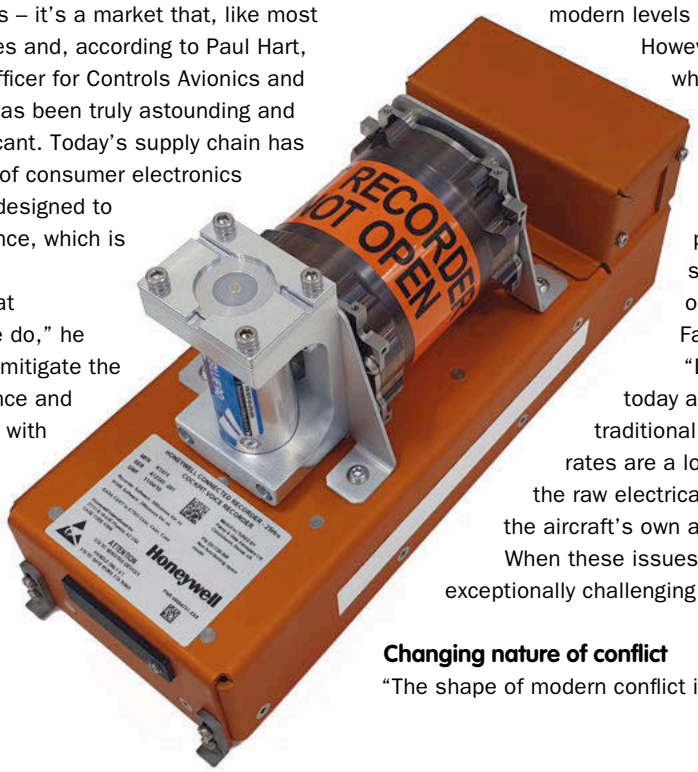
"We need to be able to install new avionics hardware and software, so we need to avoid proprietary systems.

"When you're looking to upgrade the capabilities of an aircraft that may have been designed and manufactured in the 1980s or 1990s, it's a challenge – but not an insurmountable one.

"These aircraft will not be able to meet today's military requirements and need to be upgraded. They have to be able to support electronic support measures, synthetic vision capabilities, have the ability to operate night and day and to operate safely in commercial airspace," explains Hart.

"If you want to upgrade the avionics – and the existing system is likely to have been as finally tuned as a Swiss watch – one solution is to overlay the legacy system with a new network that not only boosts capabilities but is able to pull data from the legacy system itself," according to Hart.

"Your aim is to enable that network to support and provide modern levels of performance."



However, there are just as many challenges when you are designing a modern aircraft.

"Today's designs use composite materials so that the avionics now have to be able to deal with EMC protection and possible lightning strikes, which were less of an issue in older designs – which were essentially Faraday cages.

"EMC/EMI protection is more stringent today and fibre optics have replaced traditional forms of wiring. Data and processing rates are a lot faster too, and in today's aircraft the raw electrical power supply has to be managed by the aircraft's own avionics," says Hart.

When these issues are combined it makes for an exceptionally challenging design environment.

Changing nature of conflict

"The shape of modern conflict is changing too, so the military needs

to be able to easily adapt its weapons and systems," says Hart.

In today's battlefield connectivity and interoperability are necessary requirements.

"Data collection and dissemination are critical and there's a requirement to relay information in real-time to other assets, both in the air and on the ground," and Hart makes the point that, "we are in a world that is now largely about asymmetric warfare, so systems designed 10-15 years ago need to be upgraded to meet new requirements."

Hart also makes the point that today's conflicts tend to involve multiple nations.

Paul Hart

With a long history in avionics - and spells at Thales, Smiths and Cobham, Hart joined Curtiss-Wright in 2011 as Director of Avionics Engineering. He was promoted in 2013 to Chief Technology Officer for the Avionics & Electronics Group, and then appointed as a Curtiss-Wright Technical Fellow in 2015.

"In those situations, communications systems must be able to interact with one another so that they can relay tactical data and communications."

According to Hart, "The growing use and deployment of autonomous vehicles means that communications will be critical and networks will need to be capable of processing vast amounts of data."

Military planners are always looking to improve and enhance force capabilities, giving their military the tactical edge over adversaries, and the pressure is on design engineers to square specifications with a workable and capable solution.

When it comes to drones, for example, while they are nothing new when it comes to their use by the military, they are evolving at pace and according to Hart, will see the growing use of artificial intelligence and robotic platforms.

"One of their main uses will be in surveillance and they can be deployed for reconnaissance, gathering intelligence from the battlefield before soldiers are deployed. Likewise, the use of autonomous vehicles in the field – in terms of delivering supplies – will be extended, but that will depend on developments in battery technology."

Curtiss Wright has a close working relationship with defence and research organisations, like DSTL and Innovate in the UK, and is involved in looking at how technology is likely to evolve and how it might be deployed.

"The use of augmented reality and how data and intelligence is made available to the end user is going to be critical," according to Hart. "Much of this is actually being driven by innovation in the gaming industry. Interestingly, the growing use of technology is raising issues around weight as more technology is deployed."

The use of open systems and COTS also raises concerns for military planners in terms of security, according to Hart.

"While avionics architectures have tended to be locked down, the evolution of more connected aircraft will introduce risks if the security levels of wireless networks are able to be breached – most manufacturers, operators are fully aware of this.

"Beyond avionics though, there are certainly high risks, especially as the military looks at edge processing and at addressing growing bandwidth issues.

"If a device is brought down or lost – a UAV, for example - it's quite possible that detailed tactical and security data could be lost. How do we control that – it's a huge risk going forward."

According to Hart, when it comes to obsolescence, it's critical that industry looks at upgrading legacy equipment with the necessary cybersecurity features that are capable of meeting evolving protocols and standards.

"It's not just weapons that are vulnerable but position, navigation and timings systems and, if your security is compromised, there's a real risk that all platform linked systems will be made vulnerable."

At the Consumer Electronics Show (CES), carmakers decided the way forward for dashboards was to extend them and, like military aircraft, project their graphics onto the windscreen as head-up displays.

Although few manufacturers want to use the term augmented reality, it represents an approach that design teams are using as they try to build greater intelligence into navigation and control systems.

Augmented reality of another kind is extending the kinds of experiments that researchers can perform on prototype vehicles at the University of Michigan's Mcity 16-acre testbed

Do robot cars dream of **virtual Jeeps**?

How simulated reality is helping to keep automated cars out of trouble. By **Chris Edwards**

in Ann Arbor. It makes it possible to enact scenarios that would be far too dangerous to risk on regular roads. Even under relatively benign conditions, experiments with vehicles on public highways have ended in death and injury.

Tucked away behind the university's north research complex, there is little risk of a car running over a pedestrian in the mockup of a town centre, several roundabouts and a short section of freeway. With a metal canopy simulating the RF interference properties of obstacles such as overhead bridges, the test track provides researchers and clients with a way of testing sensor rigs and higher-level controls but it is too quiet to represent the chaotic environment of real-world driving.

To bridge that gap, Professor Henry Liu and assistant research scientist Yiheng Feng of the University of Michigan have built an augmented-reality system for the vehicles. They use messages relayed by RF to the vehicle sensors to make it seem as though other cars are moving around the track with them. This lets them model situations such as another driver running a red light on the real hardware without putting the operators and other researchers on the track in danger.

Widespread communications is likely to be important to more efficient ADAS and autonomous control. At the analyst conference organised by Siemens Digital Industries last autumn, Alexandra Francois-St-Cyr, portfolio development executive, explained how the company had expanded ADAS testing to include communications. "We have been running validation using our own fleet of vehicles. With vehicle to infrastructure we could increase speed of a turning vehicle to 16mph. With just vehicle-to-vehicle, it can only turn a corner at 10mph."

Even with the help of augmented reality, testing with physical hardware remains a slow process simply because of a lack of prototypes and test tracks are limited in the range of scenarios they can support.

Although there are attempts to improve the efficiency of training AI to cope with road conditions, automakers for the moment are resigned to putting their designs through millions of miles of driving. A report by Tirias Research claimed estimates for training neural-network models for automated driving range from 10 billion to 20 billion hours of driving. "This alone would require hundreds of years to accomplish in the real world."

Above: The development of autonomous vehicles requires situations to be modelled via simulation

Moving into the virtual domain

Moving much of the process into the virtual domain entirely makes it possible not just to test multiple systems in parallel, as long as you have the server capacity to support it, but create many more scenarios. Companies are using a variety of mechanisms to build those scenarios, even turning to gaming technology in some cases thanks to its pursuit of presenting virtual reality to humans.

In the late 1990s, Epic Games developed its UnrealEngine for use in the first-person shooter Unreal

but chose to license the software to competitors. Unity Technologies followed suit in the mid-2000s and both companies have since pursued applications outside gaming, from surgery simulation to designing city infrastructure.

Around five years ago, while finalising his PhD at the University of Barcelona, Germán Ros started work on an autonomous-vehicle simulator called Synthia but after Intel expressed interest in seeing the work being applied more widely converted the software to run on UnrealEngine so that it could be distributed as open source.

Today, CARLA has close to 2000 users across academia and industry and is the basis for an annual driving challenge. Participants upload their autonomous driving agents as Docker images so they can be run on any cloud server. The agents run through scenarios based on pre-crash information compiled by the US NHTSA to try get to a programmed destination without incident.

Last year's challenge saw competitors run through more than 6000km of driving across ten Amazon Web Services nodes, each armed with eight nVidia K80 GPUs. The number of infractions, including several collisions with pedestrians and twenty with other vehicles, underlines the importance of doing this work in a virtual space. Ros sees the open-source nature of CARLA being important because it supports customisation.

Yao Zhai, automotive product manager at Unity, says programming interfaces to the company's gaming engine are vital for the engineering users. They make it possible to integrate real-time from simulated sensors and ECUs. "The Unity engine is designed in a very open and flexible way so that it is able to accommodate many of these non-gaming requirements through plugins and extensions, without changing the engine. However, the Unity engine is also evolving constantly to adopt requirements if we believe the change may benefit our broader user base across industries."

Vehicle simulation

Although engineers such as Ferenc Pintér, product lead for the Alsim tool at Almotive, have worked with game engines, the autonomous-driving specialist decided to build its own simulator to support its vehicle development and to offer to other teams.

"We know how these game engines work internally but their primary purpose is to generate visuals for the human eye, with effects such as lens flare. In self-driving cars we are giving control to the machine," he says.

With machine-vision systems, the images presented to the computer look radically different to the typical 3D scenes game engines create. The image sensors use fish-eye lens to capture as much of the surroundings as possible. They also have far less dynamic range than the human eye, which can make a dramatic difference in whiteout conditions or during nighttime.

"You need to be able to control the parameters that make the simulation look close to what the real sensors would perceive. We also want to support situations where you don't need the full visuals and work much faster on laptops if they don't need the complete stack," says Pintér, who notes that a visual simulation may use on the order of ten GPUs to render everything for a full sensor suite.

"We are big believers in building digital twins with emulators to simulate large electronics systems."
Joe Sawicki

Below: Almotive has developed its own simulator to support vehicle development

The ability to break down the simulation in simpler modules supports what Almotive sees as a vital aspect of simulation for autonomous driving and ADAS: the ability to ship software updates safely. A simulation environment makes it possible to support continuous-integration workflows without having to go through extensive hardware-based testing for each point release.

"You want to make sure it works before it gets to the vehicle. As developers send in their code, the simulation can see if they have broken anything using incremental software validation," Pintér explains. "We want to make it something you can test again and again, and quickly identify whether the error comes from simulation or the ADAS or self-driving code."

The PAVE360 environment created by Siemens provides another route to simulating ADAS in lifelike conditions and is using it to help prototype not just software but hardware controllers. Following its acquisition of Mentor Graphics in 2017, the German engineering giant has integrated the emulation hardware used to test out chip designs at higher speeds than are possible with pure software simulation before they make it to the fab. Joe Sawicki, executive vice president of IC EDA at Mentor, says: "We are big believers in building digital twins with emulators to simulate large electronics systems."

Under pressure to deliver safer systems without hurting development lifecycles, vehicle design teams seem likely to continue to exploit both simulation and hardware acceleration.

Future-proof products for demanding Automotive Applications

Using soft-termination capacitors with classic layer construction is the most future-proof method to be aligned with the failsafe strategy. Here, the available space is best utilized and simultaneous high mechanical robustness is assured. This makes it possible to manufacture resistant and high-capacitance components in small case sizes.

Construction of a standard class II automotive MLCC

Ceramic layers are usually printed with a nickel paste (electrode) and then stacked on top of each other. The capacitance is determined by the ceramic material, the electrode's arrangement and the number of layers. Subsequently, a copper layer is added to the termination, which connects the electrodes and ensures good conductivity. Compared to other manufacturers, SEMCO (Samsung Electro-Mechanics Co.) adds an additional copper epoxy layer, commonly known as soft termination. It acts as a buffer for mechanical stress and protects the more sensitive ceramic against breaking. Finally, a nickel-tin plating is added as last outer layer to avoid oxidation and to ensure solderability.

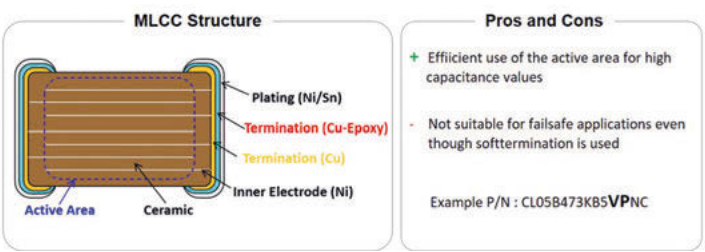


Image 1: Standard SEMCO Class II Automotive MLCC Samsung Electro-Mechanics (SEMCO

Minimize security risk

Why is the additional protection in form of a soft termination needed? What happens if the ceramic cracks? There are generally two problems. On the one hand, the insulation resistance between the layers decreases, because the ceramic material is a better insulator as a cavity. On the other hand, in the worst case, a short circuit between two opposing layers can occur. Depending on the applied voltage, this can lead to an immense thermal power loss, which can destroy the component and make the entire circuit board inoperative. For this reason car makers create their own quality standards. For example VW Group defined the VW80808 standard, which includes the "MLCC failsafe strategy". This strategy aims to minimize the mentioned security risk by setting a guideline of which products can be used in which applications.

If a short-circuit causes a power loss of >2.5W or significantly impair system function [1], the failsafe strategy must be used. This is particularly the case when battery voltage (terminal 15, 30) is applied directly to the component.

VW's standard offers four options to keep the failsafe strategy. Out of these, all SEMCO product types use a soft termination layer and are qualified according to AEC-Q200. Option number one can be used in every electric system. The other options are limited to the 12V electric system.

I. Series connection of two mutually orthogonal capacitors

The first option that can be used independently of the electric system voltage is the orthogonal placement of two capacitors in series. Image 2 shows this setup in a simplified circuit diagram.

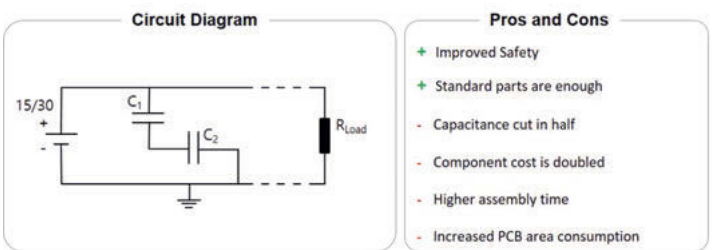


Image 2: Orthogonal Setup of two Standard Automotive Capacitors Samsung Electro-Mechanics (SEMCO)

If one of the two capacitors is placed unfavorable to bending stress, the orthogonal arrangement ensures that a backup capacitor remains intact. Since both capacitors are connected in series, the isolation to ground potential is still given.

II. Series Capacitor

A Series or "Flexisafe" capacitor uses the previously demonstrated principle of a series connection of two capacitors in a single component. The opposing layers of different potential are not directly above each other. A "floating" layer connects them.

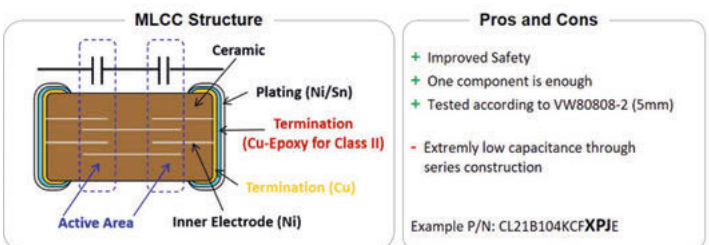


Image 3: Series Capacitor Samsung Electro-Mechanics (SEMCO)

SAMSUNG ELECTRO-MECHANICS

However, the internal structure limits the capacitance value extremely. Compared to the previous solution, not only the principle of series connection plays a role, but also the reduction of active area.

III. Open Mode Capacitor

If a crack would occur in the red marked "risky" area, it is less likely to end in a short circuit since only layers of the same potential would touch each other due to the shorter electrodes.

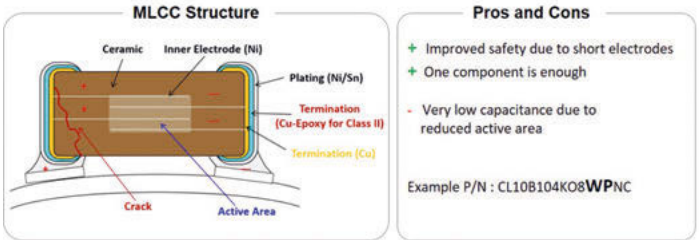


Image 4: Open Mode Capacitor Samsung Electro-Mechanics (SEMCO)

IV.Capacitor with Soft Termination

The advantages of using a capacitor with soft termination are the higher mechanical resistance and at the same time, the ideal utilization of the available component dimensions. If the layer structure is identical compared to a standard component, there is no performance gap.

As mentioned before, all SEMCO Automotive Class II capacitors have a soft termination. So, why is the standard component without this kind of termination not suitable for the use in failsafe applications? The reason is that the use of a component with soft termination is only permitted in VW Group, if it has been tested according to VW 80808-2 (Appendix A "Qualification of MLCC with soft termination"). The standard requires performing several thermal and mechanical stress tests in a row. The most critical tests are the 5mm bending ("Board Flex") and the moisture resistance test.

Standard automotive components from SEMCO are also tested according to VW80808-2, but with a bending limit of 3mm. This is above the market standard of 2mm for comparable components. The use for the automotive sector is guaranteed, but not for fail-safe applications. When you talk about soft termination in the market, you usually associate it with 5mm bending strength and the failsafe strategy. Here a differentiated approach must be done for SEMCO. The separate product family "PJ" covers the required 5mm bending strength. The qualification according to VW 80808-2 was performed here with regular criteria.

For low and medium capacitance values, additional layers of same potential are placed on the top and bottom inside the component's body. In case that the MLCC would crack, the risk of a short circuit is reduced extremely and at the same time, it results in an increased mechanical stability of the complete MLCC.

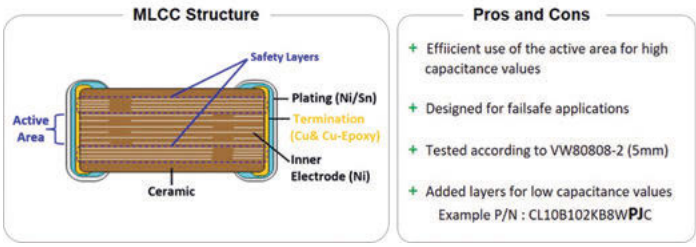


Image 5: PJ Series - 5mm Bending Samsung Electro-Mechanics (SEMCO)

For high capacitance parts, an equivalent construction to the standard articles is used (see Image 1). Since a high capacitance value must be achieved, the space is filled anyway with layers, so that the stability is guaranteed.

The soft-termination tests according to VW 80808-2 were successfully completed for all actively promoted SEMCO Automotive components.

Downsizing

The trend of miniaturization (downsizing) supports the use of the soft termination option even more. The key to small and safe components is therefore on the one hand a robust termination and on the other hand fine ceramic powder, which enables a thinner layer structure.

Product Search

The shown images highlight the part number's letters, which determine the product type (Standard, Open Mode…). To support you selecting the right component for your application, our „Product Search"-tool can be used:

http://product.samsungsem.com/mlcc/basic-search.do

Datasheets and further technical information is available here. You have the chance to filter our portfolio in terms of application, electrical and mechanical specifications.

Wasilios Pitharas

Started his career after completing a degree in mechatronics in Würth Elektronik eiSos' product management. Among other things, he expanded the product portfolio with the category "line filter". Currently he is an Application Engineer at Samsung Electro-Mechanics and responsible for technical support and business development for passive components across Europe.
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Literature:
[1] VW 80808-1: 2015-02, Page 9
[2] VW 80808-2, Appendix A „Qualifikation von MLCC mit Softterminierung"

Solving the safety **analysis problem**

Accelerated automotive fault analysis can improve more than just time-to-market, as **Jamil Mazzawi** and **David Kelf** explain

In addition to the standard integrated circuit development process, automotive semiconductors must undergo the additional burden of proving that they operate safely. However, showing that these devices operate within an acceptable level of risk, as depicted by the ISO 26262 automotive functional safety standard, can add months onto their development schedules, a significant factor given today's highly competitive automotive market.

The reason for this lengthy process is each device must undergo an analysis to demonstrate that a fault inserted into a location that could cause a critical malfunction will, in fact, not alter the execution of the device. The problem is that to date the only solution able to perform this analysis revolves around the use of a traditional fault simulator.

This 30-year-old technology designed for evaluating manufacturing tests, a totally different application, is laboriously slow. Consequently, producing the necessary metrics to satisfy the ISO 26262 measurements requires months of tool execution, delaying device delivery. Worse still is the fact that the measurement produced is the bare minimum necessary to demonstrate safety.

The automotive semiconductor market is expected to grow to $50billion by 2022, according to market research from MarketsandMarkets and, as such, represents a huge opportunity for Electronic Design Automation companies looking to solve the safety analysis problem. This has attracted considerable investment in tools and methodologies, leasing to a new wave of development tooling. New fault analysis technology looks set to dramatically accelerate ISO 26262 analysis, shaving off those potential months of painful delivery delay.

The advent of new verification techniques, such as formal verification tools, accelerated parallel simulation algorithms, and fault optimisation technologies has been combined to create a new method to perform fault analysis. This new approach can accomplish the same analysis as traditional fault simulation orders-of-magnitude faster. Indeed, in recent benchmarks it has been shown that these tools can process a complex design more than 100X more quickly, all but eliminating the month(s) long fault analysis process.

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Jamil Mazzawi is CEO, Optima Design Automation

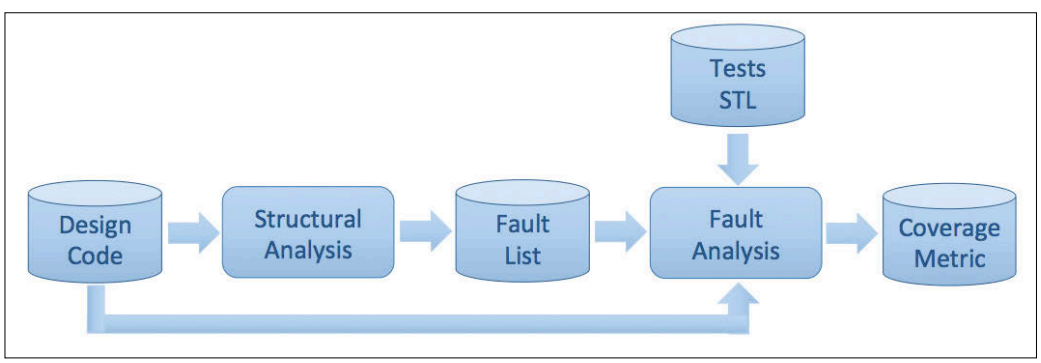

Figure 1: Traditional Fault Simulation Process

What is interesting is that the use of this new fault analysis technology has introduced new opportunities, which ensures a far greater degree of safety while also simplifying the entire development effort.

For example, traditional fault simulation relies on the fact that most fault types can be approximated, for the sake of the analysis, to a simple fault model where a signal is permanently either stuck-at-0 or stuck-at-1. This is fine for manufacturing tests, but does not describe the full story for automotive faults. For this we need to consider where these faults come from.

Environmental effects

In any semiconductor there is the possibility that environmental effects will change a bit value in a digital circuit. Electromagnetic radiation from the sun or heat from an engine has the potential to cause this problem. In most semiconductors this might require a device reboot at worst and as it happens so rarely this is not an issue. Of course automotive is different as a device failure could result in injury or worse.

A typical metric used to describe fault regularity is the Failure-in-Time, or FiT, rate, which is defined as one fault in one billion hours of operation. The highest risk tolerance level, known as ASIL-D, requires a FiT rate smaller than 10, or one fault in 100 million hours. This seems like a high number but when one considers the number of cars on the road that might use a specific device, the number does not seem so large. Radiation from the sun can produce a significantly larger number of faults than suggested by this metric.

The other issue is that a bit flip caused by radiation is often transient in nature, in that the fault appears briefly but the bit is then over-written through normal operation, eliminating the fault. These transient faults are not effectively modelled by the

standard stuck at 1/0 model, and as such may cause behaviour that would not be detected by traditional fault simulation. Even with a FiT rate of 10 or less, these faults have the capacity to send a car off a road.

A standard method to effectively eliminate transient faults requires replacing the flip-flops in a design with a more complex flip-flop component that more-than-triples its silicon area and power consumption, a process known as "flip-flop hardening." In devices where transient faults are an issue, design teams often take a "sledgehammer to crack a nut" approach and simply harden all the flip-flops in the design, dramatically increasing the power consumption in devices where power usage is a significant factor.

The analysis of transient faults across a system may be accomplished using an iterative fault analysis approach. This involves running the analysis many times. With traditional fault simulation techniques the cost of these runs is prohibitive. However, with the dramatic reduction in fault analysis time afforded by new tools, it is now possible to perform an analysis, which can lead to the replacement of just the flip-flops necessary to render the device safe.

Architectural vulnerability factor

To understand this approach, another metric, the Architectural Vulnerability Factor (or AVF) must be used. The AVF for a specific flip-flop is defined as the probability that a one cycle bit flip on that flip-flop will reach the output, and it is dependent on such factors as the probability of the bit having an unsafe influence, logical masking of the bit as it propagates through the system, etc. The overall FiT rate of the entire system may be approximated using the sum of the AVFs of the hardened flips-flops plus the AVFs of the regular flip-flops, calculated using fault analysis. By iteratively changing which flips flops are hardened, the optimum solution may be reached. Typically this will have a power consumption far less than the version where all flip-flops are hardened.

This is an example of the kind of analysis that may now be performed with this next-generation fault analysis. High-performance fault analysis may also be useful for related verification topics. For example, assessing coverage issues in a device can be very time consuming and problematic. Iterative fault analysis can be used to automatically track areas of the device for which test coverage is low, indicating a need to apply specific tests for this area or increase testing in general.

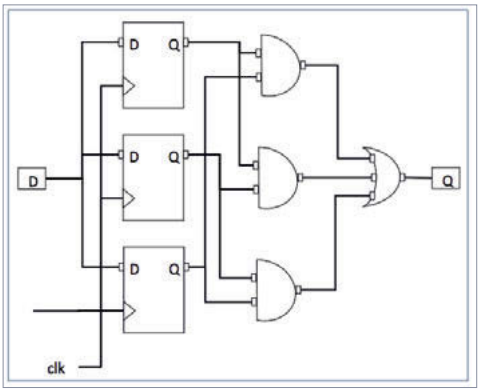

Figure 2: Hardened Flip-Flop

Using fault analysis, it is possible to insert faults and see if a testbench will pick up the change, thereby indicating if the area where the fault is inserted is effectively covered. Tradit5ional fault simulation is too flow, in general for this, but high-performance fault simulation can uncover untested items very quickly, leading to a more thorough verification process.

Fault analysis is at the root of most automotive safety verification processes, and the use of traditional fault simulation design for manufacturing test has led to overly slow safety metric evaluations. By improving fault analysis it is clear that this phase of automotive IC development becomes a lot faster, shaving months of device time-to-market. However, what is less clear is the additional functionality it provides, for example the ability to test for more complex fault models and perform automated coverage inspections. The use of high-performance fault analysis not only increases competitive time-to-market but also increases design quality and safety.

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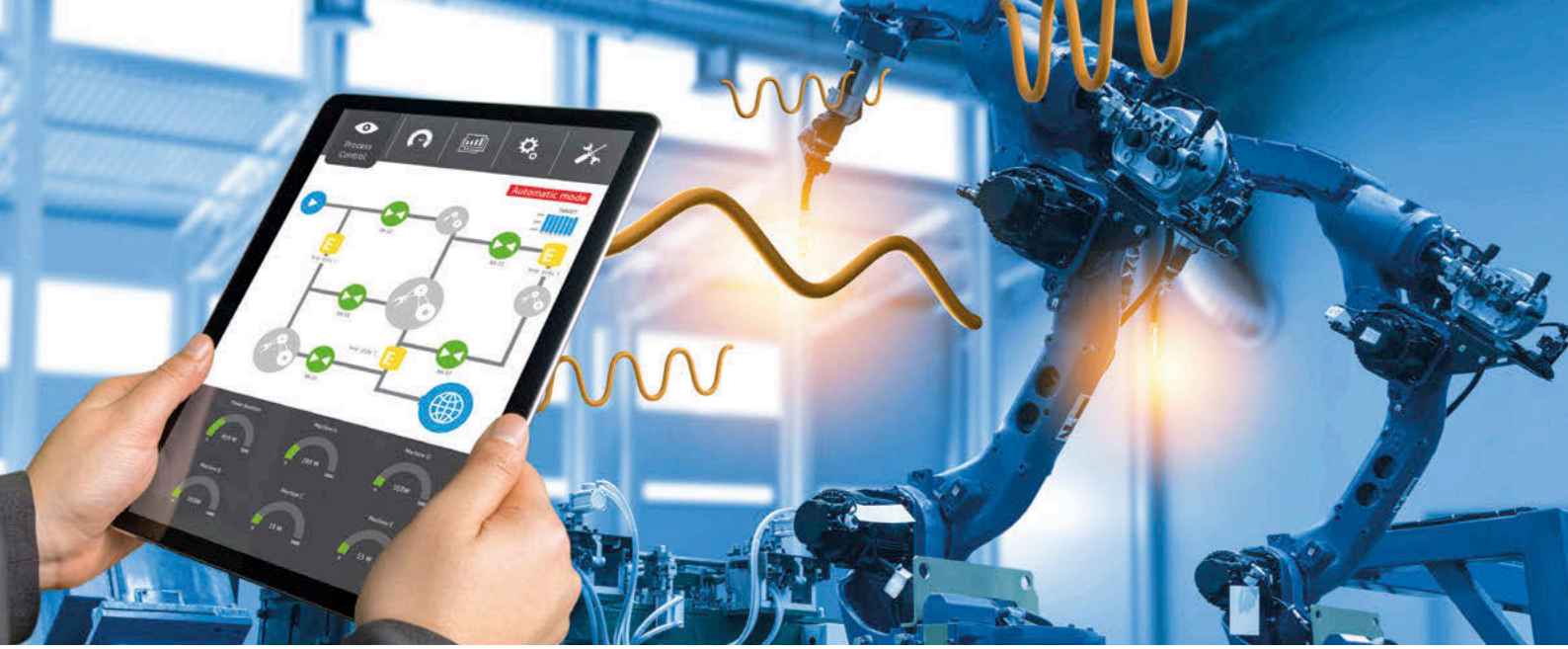

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With 4K and 8K displays hitting the market, how can manufacturers continue to improve picture quality? By **Elliot Mulley-Goodbarne**

Do you know your LEDs from your LCDs? How about the pixel pitch of panels or the projected picture on partitions for presentations?

I'd hazard a guess that such technologies do not cross your mind when setting up in a board room, sitting down in your living room or looking up for a live replay at Wembley but, in certain scenarios, you may see a change.

Getting the sharpest display has been the focus of the likes of Samsung, Sony and TCL for years now and, as mobile devices develop the capacity to record in 4K resolution and broadcasters invest in ultra-high definition channels, the technology used to view such broadcasts is in increasing demand.

But we need to start off with a disclaimer: a 4K display will not always give you a 4K experience.

Strange to say, but the human eye can only see so much detail so, for a large format display (LFD) manufacturer like NEC, the pursuit of higher resolutions is somewhat futile.

"If we were to take our 0.9 pixel pitch display you are going to need a 330 inch diagonal display to get an 8K image" said solutions sales manager Mark Taylor, "that's the problem. It needs to be for the right audience.

"That's all dictated really by how far away people are sitting and what they need to see. The whole argument when it comes to a 4K screen is 'how far or how close you'll actually be sitting', because there is a point, whether it's 4K or HD, you're not going to see any difference.

"The same goes for LEDs. You can only get the benefits of 4K if you're sitting close enough so, if it's for a general auditorium or advertising at a train station, for example, you don't need that sort of resolution."

Being an LFD manufacturer, resolution is not a concern for NEC. Granted getting the clearest picture is a priority but, as Taylor says, picture quality is only useful if it can be appreciated.

Above: With the move from lamp to laser technology, projection has become a more appealing solution for immersive content

To appreciate the resolution, you need to be a certain distance away in relation to the distance between pixels. In other words, to find the minimum, optimum and maximum distance in metres someone has to stand to be able to read text and watch video off a screen, installers have to multiply the pixel pitch by 1.5 (minimum), 2.5 (optimum) or 6.5 (maximum) respectively.

Such calculations hold firm when it comes to slightly smaller LED displays. At Integrated Systems Europe (ISE) last month, Sony unveiled its Crystal LED technology which boasted a 4K by 2K resolution on a 4.8m by 2.7m display.

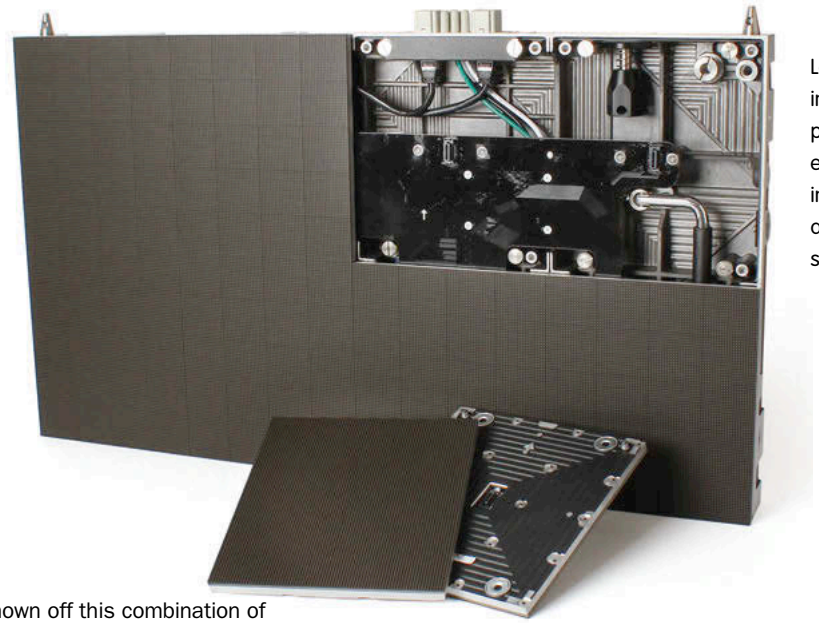
"The difference from the other LED panels is that the contrast ratio is 1 million to one" explained Sako Kageyasu, product marketing manager at Sony, "Other manufacturers have ratios of several thousand or 10,000 to one but our system is based on unique technology.

"We have our own factory building LEDs from chip to panel allowing us to eliminate extremely small areas of the display that cover less than 1% of the surface, its physical size is 0.3 square millimetres.

"At ISE, we wanted to demonstrate the technology in an application. We combined our interactive technology and put in a Kinect sensor to capture the movement of the audience and some of the interactive content."

Kageyasu said that such applications of LED technologies and sensors are being worked on in the entertainment industry with the basic principle of eliminating the need to touch a screen by using motion instead.

In the world of retail, Sony has



Left: Panel display installations have proven to be expensive but, once installed, they're a more affordable solution

shown off this combination of technology in Asia on a digital signage system that allows audience members to view themselves on screen and to interact.

According to Rob Meakin, senior European product marketing manager for LCD Projectors at Sony, the ability to blend projections into one immersive experience is becoming more appealing to retailers as well as in spaces like museums.

"Both want to do digital AR. We have the ability to blend multiple projections to create this kind of entertainment for children's museums and museums showing digital art.

"We see this in retail as well, but you do have a brightness issue to consider. Laser technology has the ability to last much longer, 20,000 hours for us with only 30% decline in brightness, not 50% which used to be the standard in brightness when it came to the lamps.

"Many manufacturers claim that their projector is protected to go for 40-60,000 hours. Sony's can last for 80,000 hours, but the brightness level after 80,000 hours is probably not really fit for the application or for the environment the projector is operating in. But providing, cost effective, large display with edge blend, multiple projection in that retail and kind of museum entertainment is becoming more and more popular."

Maintaining quality

With laser projection technology the quality of the picture has improved with Panasonic showing off a tri-laser RGB set up on a black canvas to improve the contrast output.

However, Taylor pointed to a reliance on a dark environment to get the best results as one of a number of concerns.

"In the retail environment, projectors will need to be on continuously for a long time, and that's a challenge. You have a maximum life of 20,000 hours which is a couple of years. Then you have the issue of maintenance - some sealed optical engines do need regular maintenance. Finally, brightness levels are a concern because most retailers want a bright environment."

Health and safety concerns are another issue, with Taylor citing potential retina damage if someone walks in front of a projector that is too bright.

Turning to the future, how will displays improve? Meakin says that, when it comes to Sony's projection R&D, "the number one issue will always be colour clarity and producing the correct image."

On the panel side Taylor says that improvements in picture quality have obstacles to overcome.

"You can only get the benefits of 4K if you're sitting close enough so, if it's for a general auditorium or advertising at a train station, for example, you don't need that sort of resolution"
Mark Taylor

"There are limits when it comes to pixel pitch at the moment. We are going to have a 0.9 [pixel pitch], other manufacturers have a 0.4 but when you start going down that route you're getting into the realms of cost. For a 0.4 you're probably looking around £14,000 pounds a square metre.

"The industry is starting to use other technologies like mini LED, flip chip and four in one to bring those pixel pitches down but, again, they are cost prohibitive at the moment."

Taylor adds that those high prices are due to the manufacturing costs of screens; the attention to detail needed in setting up displays; as well as the necessity to source diodes from the same manufacturer, or bin, to ensure consistent colour shades.

"When you manufacture screens, we make a guarantee there's the same shades of the red, the green and the blue. So you can get top tier diodes for a screen from us for £50,000 for instance. You might get a Chinese manufacture offering what appears to be something very similar at half the cost, but because that cost is loaded into the diodes, they'll get something from a different vendor but the colours won't be quite the same which means after years, because diodes degrade, there will be a mismatch and a significant drop off in performance.

"Diodes are expensive, the manufacturing process is expensive and shipping them is expensive as is installation.

"It's not just about hanging a screen. You need special installation crews to make sure that the structure that they go on is flat. To give you an idea, to ensure that a hundred and 10 inch screen, which is probably one of the smallest ones, is hung on a wall that is flat you're looking at between £2,000 and £3,000 in costs.

"So this is where all the costs come from. But once it's in and it has got through its bedding in period, it could be rock solid for years. They don't have to worry about it."

Looking to a secure future

Connectivity requires devices to be secure and that starts well before a device is shipped to a customer, as **Paul Karazuba** explains

As connected devices have proliferated across homes, organisations, and cities, the range of vulnerabilities has grown as well. Device security must be a primary requirement for any connected device manufacturer, and that requirement starts well before a device ever is shipped to a customer.

Any connected device can potentially become the target of attacks by nefarious parties; whether to steal personal data or intellectual property, obtain authorisation credentials for accessing connected servers or systems, or to corrupt its functionality.

All of these can be done covertly, for example as with the Stuxnet attack – which intended to sabotage uranium refining by subtly changing centrifuge speeds whilst falsifying instrument readings – or in more overt ways such as shutting down essential infrastructures or interfering with the controls of a connected car.

Take a smart city, for example; ideally a place designed to provide ultimate comfort and efficiency for citizens, Smart City deployments with neglected security can provide serious safety risks, including identity theft, ransomware attacks, and sabotaged infrastructure, such as power grids, water supply and traffic control.

Given the potentially high consequences of security breaches on IoT devices, it is startling to think that device security is often not a primary design goal of device makers.

In attempting to address these issues, governments around the world have introduced legislation focused on improving the security of IoT devices.

New regulations such as the California IoT law which came into effect on January 1, 2020 and EU regulation introduced in 2019 are now putting the onus back on the manufacturer to deliver secure devices to businesses and consumers.

Approaching device security

To meet the new regulatory requirements, it ultimately comes down to manufacturers putting security at the top of their agenda, taking a "secure by design" approach to the development of their devices.

"Secure by design" means security is treated as a primary design parameter in the development of a product. This means building security into products, starting in the design phase. Proper security starts at the chip level and extends all the way to field deployment and even end of life, using well-researched cryptographic building blocks, applying secure software development practices, and building security into your manufacturing process as early as possible.

This holistic approach means that the entire IoT ecosystem will become less vulnerable to malicious attackers – not just the individual device. It also means that it should be easier for those managing the systems to quickly detect any inconsistencies and threats before there is any opportunity to cause significant damage. The goal would be that once an attack is detected, the system should immediately be able to isolate infected devices to contain the attack, and fix the vulnerability by patching affected devices.

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Looking at hardware

"Secure by design" devices must be developed to be individually identifiable and connected. This ensures that there is an auditable path between the device and the organisation. This is essential in order to trust the data received from IoT devices sufficiently to use it in critical business decision making processes. Making this happen should take place at the hardware level, ideally with a root of trust.

Having a hardware root of trust, containing a digital ID certificate or cryptographic identifier, enables an end-to-end trusted path. The root of trust acts as the foundation for many layers of security; from the detection of new devices being attached to a system and subsequent remote service provisioning, to patching and in the case of a compromise, the isolation or blocking of devices or groups of devices.

In end devices, the immutability of hardware – as opposed to software or firmware that are frequently updated and patched (and hacked!) – provides a firm basis for identifying the device, securing the boot process, validating firmware updates received across the network, and securely storing, encrypting and decrypting data using industry-standard cryptographic algorithms executed in dedicated accelerators.

How it can be achieved?

Hardware security can be implemented in a dedicated IC, also called a secure element, acting as a companion chip to the main processor. However, deploying a dedicated secure processor as part of the main CPU is a choice that an increasing number of security-conscious device makers are making.

This permits the primary CPU to be optimised for high performance, low power consumption, or other desired characteristics, while allowing secure processes to be run in the secure processor.

Hardware root of trust products, such as the CryptoManager Root of Trust, developed by Rambus, provide system designers a method of deploying secure processes and applications. They often contain a series of hardware engines coupled with a secure processor designed to provide services to the main processor, including secure boot and runtime integrity checking, remote authentication and device attestation.

Figure 1 below, demonstrates the CryptoManager Root of Trust. The hardware also typically performs key derivation, which enables key strengthening and improved secrecy.

Proper protection at the silicon level must also include anti-tamper mechanisms to block attacks such as bus probing, fault injection, and over-clocking. It can also incorporate logic and crypto redundancy, secure-state encoding, and ephemeral keys that are generated on the fly from multiple splits and flushed immediately after use. In addition, root of trust cores should feature an entropic array with a proprietary logic structure that provides robust protection against emulation and reverse engineering.

Author details:
Paul Karazuba, Senior Director, Product Marketing of Security, Rambus

To ensure robust protection, the root of trust hardware depends on associated security services that must cover the complete device lifecycle. One of those associated security services is device provisioning and key management. Device provisioning involves the injection of secret keys or other device identification data into the device; ideally, this is done at the silicon level during the silicon manufacturing process. Incorporating a dedicated provisioning infrastructure as part of this establishes the trust chain at an early point in device manufacture.

Key Management Services enable the device maker to authenticate and attestate devices anywhere in the world. Through a secure connection, these services allow the device maker to monitor device status, "roll" cryptographic keys, provide disaster mitigation and recovery services, and even decommission devices, reducing the risk of devices being hijacked, copied, re-purposed, or disabled. Compromised or cloned devices can be quarantined and recovered. Protection against cloud-based threats such as DDoS, cross-site request forgeries and digital offensives against unprotected REST APIs should also be included.

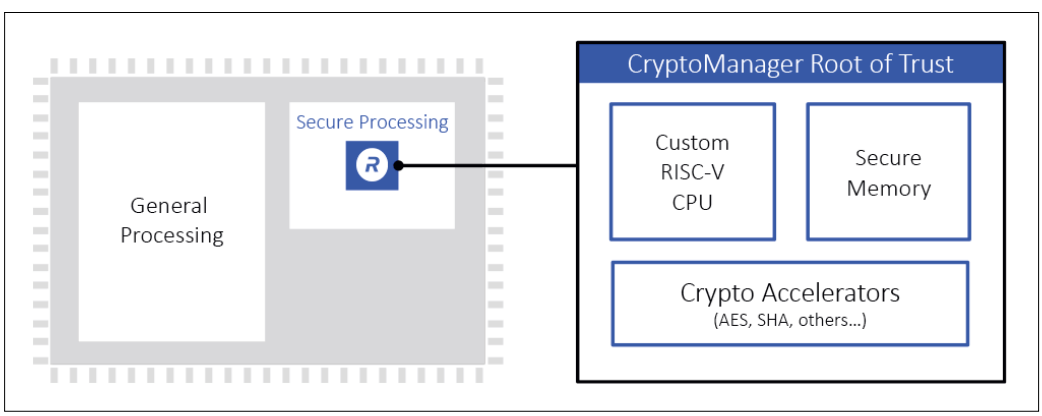


Figure 1: CryptoManager Root of Trust

Security and profitability

With the introduction of "secure by design" principles, we should start to see manufacturers moving away from neglecting device security. In the modern world of IoT, businesses and consumers are becoming increasingly aware of security pitfalls in products, so for a manufacturer to see profitable success, it will become essential that security is front and centre in device development.

THE AIOT 'BIG BANG'

With billions of devices, using zetabytes of data, coming to market a new class of processor looks to meet the demands of the growing AIoT. By **Neil Tyler**

With devices getting smarter and intelligence now becoming an essential element in homes, vehicles, and workspaces, what's referred to as the Artificial Intelligence of Things (AIoT) is fast becoming a fact. According to market research, by 2025 there is expected to be 65 billion connected devices generating 180 zetabytes of data, all of which will require complex and diverse processing capabilities.

That brings with it a number of challenges for design engineers who will have to address problems such as speed, reliability and security. The growth in the AIoT will also see more AI-enabled decisions taking place on-device as opposed to in the cloud which is energy hungry and expensive.

Too many of today's smart products are reliant on processing in the cloud and the growing adoption of natural voice interfaces, imaging and presence detection, for example, not only raise performance issues but will create further challenges in the form of reliability, privacy and cost.

In fact, as voice control becomes mainstream issues around latency will be exacerbated as the number of connected devices grows.

"Device proliferation and the growing diversity of demands means that there has been a need for a new type of processor," suggests Mark Lippett, CEO of XMOS, the Bristol-based fabless semiconductor company behind voice solutions, audio products, and multicore microcontrollers.

"There is a huge market opportunity for a device that is able to address the needs of a range of applications delivering both performance and functionality while, at the same time, offering ease of use, low power and real-time operation.

"This is a space that's dominated by performance and price and there has, and will remain, a necessary process/performance trade-off that will need to be addressed. What's required is the ability to match the features of a processor to the requirements of the end product and then ensure that it's affordable," he explains.

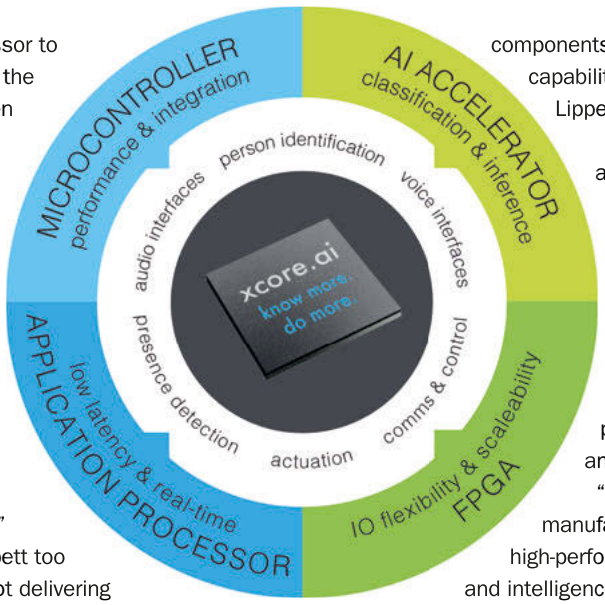
Lippett makes the point that there's no point in coming up with a solution that costs too much to be deployed. "First and foremost, you have to keep a very careful eye on cost."

According to Lippett too many devices are not delivering the levels of performance needed.

"Devices increasingly need to be on all the time, so power management is critical. But there's also a third comparator," according to Lippett, "and that's the growing diversity of customer demands. That is making it increasingly problematic for companies who are looking to differentiate their products in what are becoming commoditised markets, especially those that lack the necessary flexibility to address dynamic markets that require products getting to market quickly."

The company's xcore.ai is its response to this fast developing AIoT market and it has been designed to deliver high-performance AI, DSP, control and IO in, critically, a single device.

"To date these types of capabilities have tended to be deployed either using a powerful (and costly) applications processor or a microcontroller with additional components to accelerate key capabilities," according to Lippett.



Above: The processor has been designed to deliver performance, flexibility, scalability and is AI enabled

"Device proliferation and the growing diversity of demands means that there has been a need for a new type of processor." Mark Lippett

"What we've been able to do with the xcore.ai is to provide a crossover processor that can deliver real-time inferencing and decision making at the edge, as well as signal processing, control and communications.

"This will enable manufacturers to integrate high-performance processing and intelligence economically into their products."

The device employs deep neural networks that use binary values for activations and weights rather than full precision values, which has helped to dramatically reduce execution time.

"By using binary neural networks, we're able to deliver 2.6x to 4x more efficiency than is the case with traditional 8-bit counterparts," says Lippett.

A new generation of embedded platform

According to Lippett, the xcore.ai, "heralds an entirely new generation of embedded platform. We've designed it to be versatile, scalable, cost-effective and easy-to-use."

Fast processing and neural network capabilities means that the xcore.ai can process data locally, within nanoseconds.

"In the evolving AIoT ecosystem, that capability means that manufacturers can build smarter

sensing technologies that will be able to fit seamlessly into smart devices," Lippett explains. "Not only that, the xcore.ai is delivering, what we believe, is record processing power at the dollar price-point. That means electronics manufacturers, whatever their size, will be able to embed multi-modal processing into all sort sorts of smart devices."

The xcore.ai looks to deliver solutions that will be able to address challenges associated with the AIoT, such as latency, connectivity, privacy and energy consumption, while at the same time keeping costs low and, crucially, keeping design potential high, according to Lippett.

"At XMOS we aspire to be the only digital piece of silicon in the box."

The device is flexible so that it can be used across a wide range of markets from asset tracking to personal health and well-being, as well as a host of smart appliances in the lighting, security and audio-visual space.

But what does this all mean in reality? Can the xcore.ai help to change the user experience for the better?

Lippett highlights its versatility with the example of a smoke detector.

"The smoke detector was designed to ensure our safety. They were developed over a hundred years ago but while they have come a long way, are they able to do enough?

"While they may alert us to danger and we instinctively know to exit the premises when we hear one, how can we truly optimise the smoke detector to dramatically reduce risk and support rescue and recovery?"

According to Lippett, by using the xcore.ai it will be possible for a smoke detector to deploy radar and imaging to identify whether there are people in an affected building and, if so, determine how many there are and where they are located.

"Using voice interfaces, the detector could communicate with those inside, while vital sign detection could identify whether they are breathing. Put together, this builds an intelligent picture of the environment that can be fed straight to the emergency services, enabling an informed rescue operation, improving accuracy and speed of response," he explains.

Another possible example comes with the need to develop affordable, unobtrusive and easy-to-use healthcare solutions for a fast ageing population.

"Think of a smart personal health companion that can constantly monitor vital signals giving the earliest possible indication of the need for specialist care," explains Lippett.

"Personal data is held securely on device, without being sent to the cloud, and can be shared with trusted medical or care staff through appropriate permissions. The system can even detect medical emergencies such as a fall, and take appropriate action without delay."

Scalable and multi-core, the xcore.ai processor is able to deliver improved levels of performance and enables embedded software engineers to deploy every different class of processing workload on a single multicore crossover processor that's able to interpret data without having to communicate with the cloud.

"It's fully programmable in 'C' and there are specific features such as DSP and machine learning that are accessible through optimised c-libraries," explains Lippett.

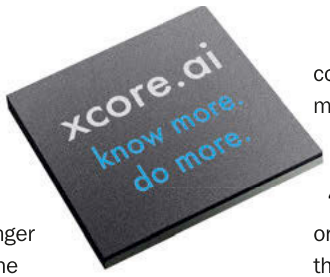
"It has 1Mb of embedded SRAM on chip, which is complemented by an LPDDR interface providing simple memory extension where required.

"It also supports the FreeRTOS real-time operating system, enabling developers to use a much broader range of familiar open-source library components. It is also compatible with TensorFlow Lite which allows easy prototyping and deployment of neural network models."

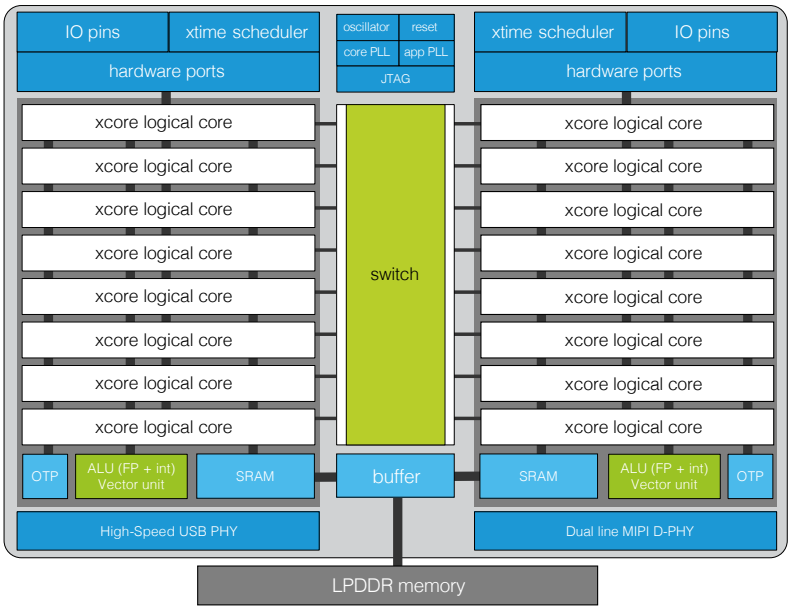
In terms of connectivity xcore.ai has up to 128 pins of flexible IO giving designers access to a much wider variety of interfaces and peripherals, which can then be tailored to the precise needs of the application.

"We've also integrated hardware, such as USB 2.0 PHY and an MIPI interface, so it's possible to collect and process data from a wide range of sensors."

"What we've looked to deliver with the xcore.ai is an economic solution that combines higher performance and flexibility with energy efficiency " says Lippett.



Above: The xcore.ai processor



Left: A block diagram of XMOS's xcore.ai processor

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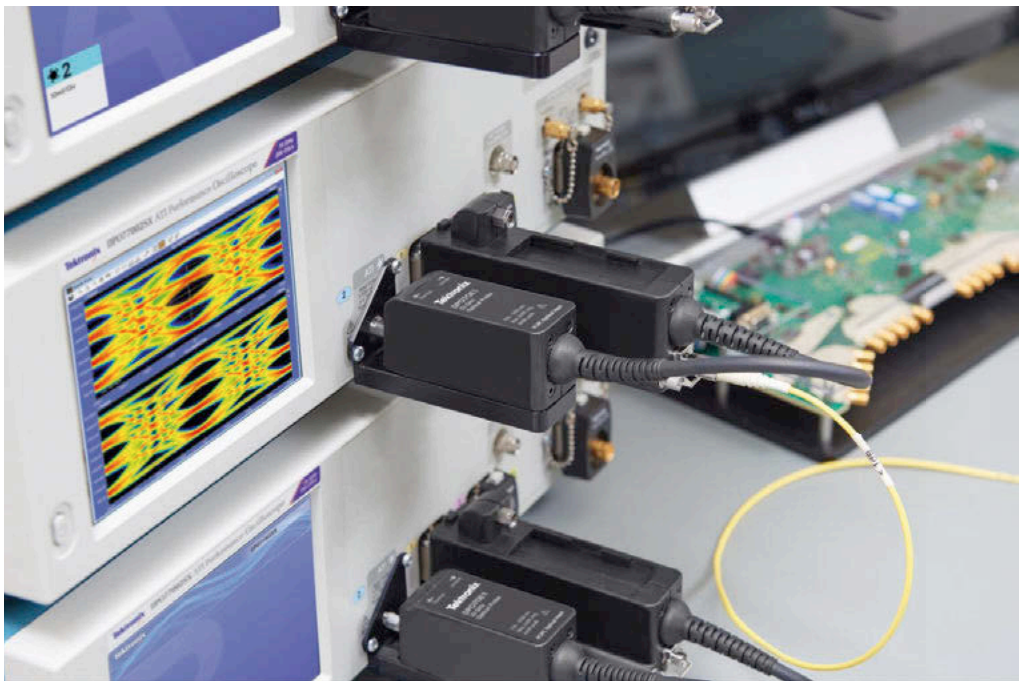


ALL EYES ON HIGH-SPEED COMMS

Ethernet is driving progress on fast links and bringing changes to testing with it, as **Chris Edwards** discovers

If there is a one protocol that has effectively taken over communications it is Ethernet. Driven by demand within and between data centres, the networking standard is moving into areas like front- and back-haul communication for high-speed wireless cellular networks. Even for systems that will not use its packet formats, the work that goes on in the Ethernet standards committees is driving progress in the physical layer for other high-speed links. This is leading to big changes in the way communications links are tested as well as presenting engineers with a dizzying range of options when they decide on which physical-layer format to adopt.

Since the idea of taking Ethernet to 100Gbit/s and beyond was first proposed the options have multiplied. They range from signals being carried over as many as 16 lanes over multiple electrical paths or wavelengths carried on a number of fibres to a single optical wavelength on a single-mode fibre.

Because of the bandwidth limitations of even high-grade copper and optical transceivers, a key change in the push to 100GbE and higher speeds is to pack more into each transmitted symbol.

Instead of classic two-level, non-return-to-zero (NRZ) signalling the IEEE 802.3bs standards committee settled on the four-level PAM4 modulation scheme for the higher speeds.

"The biggest challenge is the fact that the signal to noise ratio gets squeezed by looking at three eyes. While the data rate is doubled, the signal-to-noise ratio is halved for each of the individual eyes, which causes significant design challenges," says Brig Asay, Keysight's director of strategic planning in the company's internet infrastructure group.

One consequence of the greater susceptibility to noise in a multilane environment is crosstalk.

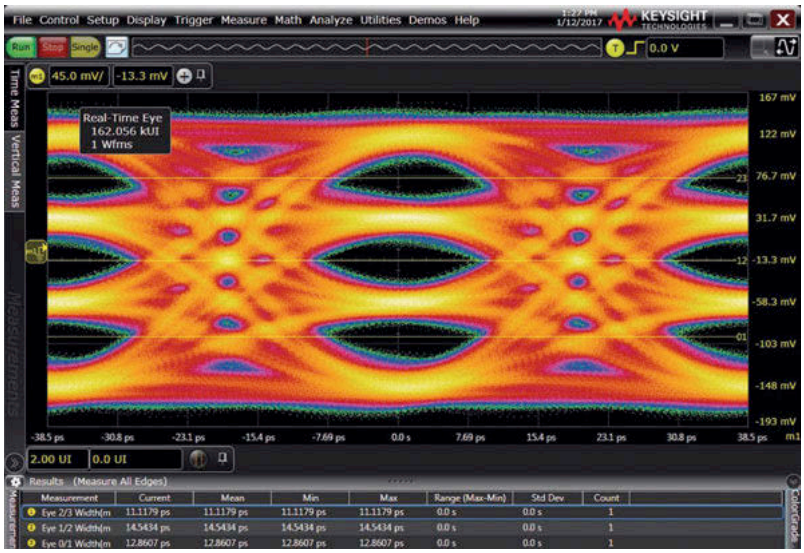
"Crosstalk is a huge pain. And the crosstalk is present in optical systems because the transmitter is not a completely optical device and you create crosstalk there, so the light you send is imprinted with that crosstalk," says Tektronix domain expert Pavel Zivny.

With three eyes to assess instead of one, engineers who need to test their transceiver and system designs have Instead of using one eye diagram to assess the quality of a transmitter, you now have three to assess. Not only that, there are a host of other more subtle measurement issues and changes to techniques that R&D teams have to deal with.

"For NRZ there was a rather simple mask test to check everything is fine," says Alessandro Messina, EMEA wireline products marketing director at Anritsu. But the presence of multiple eyes means any imbalance between them makes the conceptually simple job of counting hits inside the mask much more troublesome to execute in practice.

Zivny says the days of the mask test were close to being numbered even when used with NRZ and that a test regime defined in the 1970s is not a good fit for today's protocols.

"Now we are asking, when you measure something, do you really need to measure it? Is failing that measurement really hurting your link? With mask tests, if the voltage swings into the mask you get punished. But the end user couldn't care less about that voltage. The end user cares about errors."



Left: A Keysight shot of a PAM4 eye diagram, showing the three eyes

Standards and trade-offs

Although it did not gain acceptance for any existing NRZ-based standards, the concept of transmitter and dispersion eye closure (TDEC) provided a metric for assessing the degree to which transceivers, particularly those operating in the optical domain, are able to cope with impairments such as low-pass filtering, noise, compression and signal skew. For PAM4, standards committee adopted the quaternary version: TDECQ.

The trade-off though is that working with TDECQ involves a number of subtleties that are not immediately obvious.

One issue that the standards committees met early on was the amount of data that needs to be collected to gain insight into how well a transceiver is working as a pattern generator fires a stream of symbols into the device. The first choice turned out to take too long.

Pete Anslow, distinguished engineer at networking-equipment maker Ciena, proposed to the IEEE 803.2bs committee a more efficient pattern: short stress pattern random - quaternary (SSPRQ).

"The pattern was not completely new but he did a rigorous job of ensuring it had the right statistical properties and followed the behaviour of real traffic," Zivny explains.

The SSPRQ pattern lived up to it name: it stressed designs that developers believed should work and which passed other tests. Despite the pushback from some quarters, the pattern has been accepted as good for exercising systems.

Improved equipment informed by high-stress patterns cannot fix all the problems of PAM4. Above a distance of around 100cm, noise on the transmission path introduces errors that cause the bit-error rate (BER) to balloon from less than one per quadrillion events to one per ten thousand. Although it was present in earlier Ethernet standards but often treated as somewhat optional, forward error correction (FEC) is a vital part of the high-speed Ethernet standard.

"The impact of FEC on BER is that it takes the bit-error rate from 10E-4 to 10E-15," says Asay. "It also adds a level of complication to debug as now designers must see why their FEC has failed."

FEC is sensitive to the distribution of errors, Zivny says. Burst errors can kill a block while periodic errors that affect only a few bits in each block will let a link operate as though nothing were wrong. Some of the newer tests in the standard focus on this kind of problem.

Messina says there are two levels of issues that may mean using more sophisticated BER instrumentation.

"One is to be able to simulate FEC signals to understand what is the real quality when FEC is enabled. At the same time I also need to simulate jitter stress. If I can simulate both together, I can see exactly what would happen in real life. If I can't emulate FEC while jitter stress, I can only run theoretical calculations. So, it's best to be able to have both."

The second issue is handling multilane traffic. "FEC only works correctly when all channels are flowing through the transceiver. So for an eight-lane 400Gbit/s link, reproducing real life conditions requires eight channels from the BER tester."

Because of the different transition levels in PAM4, jitter measurement is more complex than with NRZ though the standards have adapted their recommendations to follow suit. Messina says jitter will need more precise tools for measurement as the transceiver hardware rolls out. Asay adds: "We continue to see new jitter measurements getting implemented for PAM4."

As 400GbE equipment moves into the market, communications vendors are beginning to look at the following generations and the possibility of a move to a higher symbol rate that might support 800GbE and above across eight or fewer lanes.

"800Gbit/s might be achievable by switching from 26Gbaud on eight channels to 56Gbaud. The question is how to go higher than 800Gbit/s. Some companies are looking at 112Gbaud as being the next step or maybe more channels," Messina says. "There may be a third option: keep the speed as it is but use different modulations, maybe PAM8."

At this stage it is not clear which way the equipment makers will move though Messina sees a reticence to increase lane count because of its effect on power consumption.

The other directions imply another phase of development on testing regimes that can exercise transceivers without making their designers jump through unnecessary hoops.

"The biggest challenge is the fact that the signal to noise ratio gets squeezed by looking at three eyes, which causes significant design challenges"
Brig Asay