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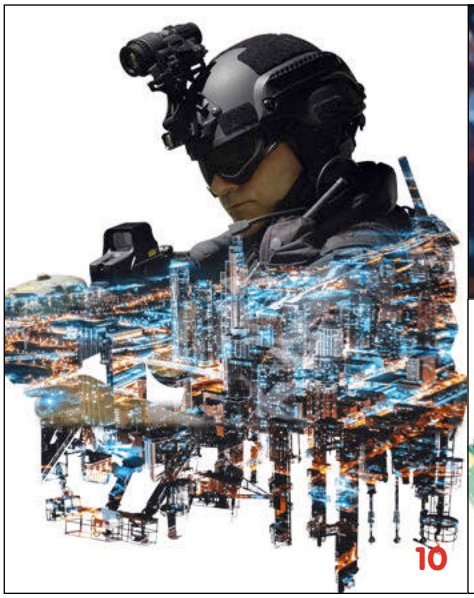

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IF NVIDIA ENDS UP BUYING ARM, WHAT IMPACT IS IT LIKELY TO HAVE ON THE COMPANY AND ITS SUCCESSFUL BUSINESS MODEL?

The rumours that Nvidia is in talks with SoftBank to buy Arm Holdings are gaining traction, so the current radio silence from both could be a clear indication that something is afoot.

Originally, SoftBank appeared to have approached Apple about selling the tech company, but that seems to have fallen through. Now the possibility that SoftBank might be selling Arm to Nvidia raises some interesting questions about its future.

Once described as the jewel in the crown of British tech Arm, which licenses its IP to the likes of Apple, Qualcomm and Nvidia itself, has always been seen as a neutral supplier, one not in direct competition with its customers.

That could be where the proposed Nvidia acquisition becomes problematic, because although some argue that Arm's IP is simply a 'commodity' and that it's the other design IP that surrounds the Arm core that holds the key differentiators, Nvidia could end up influencing Arm's future R&D direction ensuring that Arm provides it with priority access to new and future designs – which wouldn't be surprising when they could be paying over $30bn for the company.

It would also end Arm's 'neutrality'. If it is acquired by Nvidia will it be able to serve the likes of Qualcomm or Apple? How will they feel about licensing IP from a unit that's now owned by a significant rival?

Arm co-founder, Hermann Hauser, speaking to the BBC said that by allowing Nvidia to buy Arm it would compromise that neutrality and the ability of the company to address the needs of multiple disparate customers and there would be a good chance that Arm would lose many of them – in short it would be a 'disaster'.

In response, perhaps to these concerns, reports have been circulated suggesting that Nvidia may simply look to take a stake in Arm, with SoftBank retaining a share. The idea of joint ownership has also been floated, according to reports.

So if this is true and Nvidia is looking to buy Arm, what are the advantages?

Nvidia licenses technology from Arm for its Tegra chips, but these devices don't have a significant share of the mobile market so in terms of competition it seems unlikely it could be stopped on competition grounds – although any acquisition would face intense regulatory scrutiny.

Nvidia would probably use Arm's capabilities to develop more powerful chips driving higher performance levels. It's also 'unlikely' that Arm's existing customers would drop them, when there aren't really any other suitable architectures available to them.

How many of Arm's customers does Nvidia actually compete against?

Could a tie up between these two tech companies actually be beneficial, bringing together Nvidia's AI processing capabilities with Arm's power saving techniques?

There are, however, some big questions that need to be answered about this possible deal. Could Nvidia decide not to keep R&D focused in Cambridge and control everything from the US, and if Nvidia intends to buy ARM, how and where will it look to compete?

It's a big deal, with significant consequences for the industry.

Neil Tyler, Editor (neil.tyler@markallengroup.com)

"The rumours that Nvidia is in talks with SoftBank to buy Arm Holdings are gaining traction, so the current radio silence from both could be a clear indication that something is afoot."

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Making RTL verification easier

CODASIP INTEGRATES CLOUD SIMULATION PLATFORM INTO ITS RISC-V SWERV CORE SUPPORT PACKAGE. **NEIL TYLER** REPORTS

Codasip, a supplier of customisable RISC-V embedded processor IP, and Metrics Design Automation, a provider of the True Cloud EDA solution, have announced the integration of Metrics' SystemVerilog RTL Simulation Platform within Codasip's Pro SweRV Core support package.

According to the announcement, the integration will provide an easy-to-use and inexpensive way for ASIC designers to verify modifications and enhancements they make to the SweRV embedded processor IP.

One of the major benefits of the open source RISC-V ISA is that it allows users to customise their processor IP for optimal implementation in domain-specific applications. However, this comes with the responsibility to verify any changes made to the processor IP for functional accuracy. Codasip and Metrics have teamed up to address this requirement by making RTL verification available in the Cloud directly from the Codasip SweRV Core support package. As a result, SweRV and the support package users do not have to install and license any EDA software, do not have to make any expensive purchases of RTL simulation software, and have all the SweRV and verification IP required preloaded in a Cloud cluster for immediate use.

"Codasip continues to expand its ecosystem for RISC-V embedded processor IP," said Karel Masař ík, CEO of Codasip. "This integration of the Metrics Cloud Simulator in our SweRV Core support package is an example of making RTL verification easier and more affordable for Codasip customers and SweRV users."

The Metric Cloud Simulator is a fully compliant SystemVerilog simulator and is the only RTL simulator available with a SaaS business model - users simply pay for use as a service.

The implementation of Metrics simulator in the Cloud will help to provide massive scalability so regression tests can run in parallel and can be completed in a matter of hours, not days.

"The popularity of RISC-V and in particular the SweRV open source processor IP has been impressive," noted Doug Letcher, CEO of Metrics. "We are excited to partner with a leading RISC-V embedded processor IP vendor such as Codasip to deliver better usability, accelerated verification, and much more affordability of RTL simulation tools to the ASIC and SoC design community."

The SweRV Core support package with Metrics Cloud Simulation integration is now available.

MEMS Clock-System-on-a-Chip to reshape market

SiTime Corporation, a leader in MEMS timing, has announced the launch of the Cascade family of MEMS clock ICs for 5G, wireline telecom and datacentre infrastructure.

The SiT9514x clock-system-on-a-chip (ClkSoC) family, consists of clock generators, jitter cleaners, and network synchronizers that are able to deliver multiple clock signals in a system. This family uses SiTime's recently launched third-generation MEMS resonators that deliver higher performance with lower power.

Communications and enterprise electronics have previously used clock ICs with external quartz references to integrate multiple timing functions and to distribute clock signals. SiTime's all-silicon clock architecture provides more integration by integrating a MEMS resonator reference inside the package. More importantly, the Cascade clock-system-on-a-chip is able to deliver up to 10 times higher reliability and resilience, enabling the 5G vision of zero downtime.

Either standalone or together with SiTime's MEMS TCXOs and OCXOs, the SiT9514x is described as a complete timing solution that's suitable for applications such as 5G RRUs, small cells, edge computers, switches, and routers.

"Our MEMS technology is well suited to solve the difficult timing challenges of emerging 5G infrastructure. This market represents a large growth opportunity for SiTime," said Rajesh Vashist, CEO of SiTime. "The Cascade family is a natural next step for our timing business, but it also brings us closer to our customers. SiTime's Cascade devices offer a complete clock-system-on-a-chip, which allows customers to simplify their designs and reduce time to market. As the only provider of MEMS resonators, oscillators, and clock ICs, and delivering system-level benefits to customers, SiTime continues to transform the $8 billion timing market."

Addressing 5G network design challenges

ANALOG DEVICES COLLABORATES WITH INTEL ON RADIO PLATFORM FOR ADDRESSING 5G NETWORK DESIGN CHALLENGES. **NEIL TYLER** REPORTS

Analog Devices (ADI) is collaborating with Intel to create a flexible radio platform that will be able to address 5G network design challenges and help customers to scale their 5G networks more quickly and economically.

The radio platform combines the advanced technology of ADI's radio frequency (RF) transceivers with Intel's Arria 10 Field Programmable Gate Arrays (FPGAs) giving developers a new set of design tools for 5G solutions.

The communications market is moving at a rapid pace to keep up with the strains put on bandwidth and latency as more people transact business digitally and consume and transmit data from everywhere. A significant increase in traffic over existing wireless networks is occurring in both private networks and public spaces. As a result, wireless operators are looking to shorten development times and cost-effectively implement new solutions that increase the capacity, performance and reliability of 5G networks. Through a mix of open standards and existing communication links, mobile network operators are developing a broader set of specifications and supporting a growing span of use cases.

"This new radio platform reduces the overall cost of design and quickens our customers' time to market without sacrificing system-level performance," said Joe Barry, Vice President of the Wireless Communications Business Unit at ADI. "By coupling ADI's transceivers featuring advanced digital frontend (DFE) functionality with Intel's leading FPGA technology, our customers' solutions can achieve the high level of performance they require while increasing their flexibility to more efficiently resolve emerging network issues."

The high-performance, O-RAN compliant solution uses ADI's market-leading software defined transceiver, which includes an innovative DFE capability, with Intel's Arria A10 FPGA to create a highly flexible architecture. The collaboration will allow designers to customise frequency, band and power to achieve higher system performance at lower cost.

"This collaboration between ADI and Intel enables the development of new radio solutions for 5G networks," said CC Chong, Senior Director, Head of Wireless & Access, Programmable Solution Group at Intel. "We look forward to working with ADI to expedite hardware development by offering FPGA platforms that are flexible to meet changing requirements, are easy to use, and remove many of the complex barriers of RF and digital product development."

Comprehensive custom ASIC offering from Marvell

Marvell has announced a custom ASIC offering that looks to address the requirements of next generation 5G carriers, cloud data centres, enterprise and automotive applications.

Marvell's custom ASIC solution enables a broad range of customisation options and a differentiated approach with best-in-class standard product IP including Arm-based processors, embedded memories, high-speed SerDes, networking, security and a wide range of storage controller and accelerators in 5nm and beyond.

Traditionally, data infrastructure manufacturers and cloud data centre operators have had to choose between securing standard products or a full custom silicon solution designed in-house, while developing or licensing foundational IP as needed. Now, for the first time, Marvell is offering full access to its broad and growing portfolio of data infrastructure standard product IP and technologies, which can be integrated and enabled in custom ASIC solutions at the most advanced technology nodes.

"Marvell's ability to pull optimised components from across it's product portfolio adds a new dimension to what we can deliver," said Kevin O'Buckley, general manager of the ASIC BU at Marvell. "The breadth of Marvell's infrastructure technology portfolio is unique in the industry – and is available in one comprehensive offering."

Revolutionising wearables manufacture

Researchers from the University of Surrey, University of Cambridge and the National Research Institute in Rome have demonstrated the use of a circuit design that uses an alternative type of device, the source-gated transistor (SGT), to create compact circuit blocks that could transform manufacturing processes for wearable technology.

They were able to show that they are able to achieve the same functionality from two SGTs as would normally be the case from today's devices that use roughly 12 TFTs – improving performance, reducing waste and making the new process far more cost effective.

The team believe that the new fabrication process could result in a generation of ultra-lightweight, flexible electronics for wearables and sensors.

Dr Radu Sporea, Lecturer in Semiconductor Devices at the University of Surrey, said: "We are entering what may be another golden age of electronics, with the arrival of 5G and IoT enabled devices. However, the way we have manufactured many of our electronics has increasingly become overcomplicated and has hindered the performance of many devices.

"Our design offers a much simpler build process than regular thin-film transistors. Source-gated transistor circuits may also be cheaper to manufacture on a large scale because their simplicity means there is less waste in the form of rejected components and could result in future phones, fitness tracker or smart sensors that are energy efficient, thinner and far more flexible than the ones we are able to produce today."

Scientists from the Tokyo Institute of Technology and Socionext have developed a transceiver for enabling seamless communication between earth ground platforms and satellites in the low, middle, and geostationary earth orbits.

The scientists have developed a transceiver for SATCOM using standard CMOS technology. The transceiver, which operates in the 'Ka band', means a 27–31 GHz frequency range for uplink (ground to satellite) and 17–21 GHz range for downlink (satellite to ground).

The design is said to carry a variety of features. On the transmitter (TX) side, a high-quality-factor transformer is employed to achieve efficient power use and high linearity in transmission, which results in lower distortion during transmission. The receiver (RX) side features a dual-channel architecture that unlocks several capabilities.

By having two RX channels it allows for receiving signals from two satellites simultaneously. These signals are received in parallel using either two independent polarization modes or two different frequencies. In addition, the proposed design can perform adjacent-channel interference cancellation, increasing the dynamic range of the system, and allowing it to operate correctly even in less-than-ideal scenarios with stronger noise and interference.

Both the TX and RX perform direct conversion of a signal without additional intermediate frequency conversions, helping to reduce the overall complexity, size, and power consumption of the transceiver.

The scientists have created a prototype chip to test the actual performance of their design when using all the modulation schemes regulated by the SATCOM DVB-S2X standard. This includes high-order modulation techniques like 64 APSK and 256 APSK, which provide fast data rates.

The performance test results are said to be very promising, especially when compared with other existing SATCOM transceivers.

60 GHz radar chip for contactless health tracking

IMEC DEVELOPS A MMWAVE MOTION DETECTION RADAR AT 60GHZ TO ENABLE CONTACTLESS HEALTH MONITORING. **NEIL TYLER** REPORTS

imec has presented a mmWave motion detection radar at 60GHz, integrated in standard 28nm CMOS, to the recently held IEEE/RFIC conference.

This ultra-sensitive radar, with a 2-cm range resolution, has been designed for vital sign monitoring and gesture recognition. The compact radar chip consumes just 62 mW, making it possible to be integrated into small, battery-powered devices.

imec's radar design generates fast modulated waves, with a frequency increase of 12 percent in just 51.2 microseconds. A high modulation bandwidth (7.2 GHz) determines the sensor's ultra-fine resolution, which makes it suitable for 3D sensing of finger motions, hand swiping and gestures. Experiments have demonstrated the sensor's ability for multi-target detection, heartbeat detection at 5 metres and accurate tracking of a pedestrian's position and velocity.

The radar operates in the frequency band around 60 GHz, a license-free ISM band that can be used for new IoT applications for industrial and medical purposes.

The system only consumes 62mW which is significantly lower compared to state-of-the-art radars in this frequency range. A quick start-up time (1µs) supports aggressive duty-cycling for further power reduction. The 4.15 mm^2 transceiver chip is integrated in 28nm bulk CMOS technology, ensuring a low-cost solution at high volume production.

Commenting Barend van Liempd, program manager radar at imec said, "The radar enables devices to sense their surroundings, which will shape the way in which we control and use them and it will open a new range of smart applications in the context of personalised health, baby monitoring, sports, elderly care, patient monitoring, nurse efficiency or worker safety"

4D imaging radar on a chip

RFISee, a developer of imaging radars for the automotive industry, has unveiled a Phased Array 4D imaging radar on a chip. The all weather radar has proven its ability to detect cars from 500m and pedestrians from 200m, with an angular resolution greater than 1 degree.

Prototypes of RFISee's radar are under evaluation by top automotive OEMs.

RFISee's patented 4D imaging radar uses a powerful focused beam based on proprietary Phased Array radar technology. The focused beam created by dozens of transmitters rapidly scans the field of view. The receivers ensure a much-improved radar image, a better signal to noise ratio, and a detection range of obstacles such as cars and pedestrians that is six times broader when compared to existing radars.

The radar technology is also capable of dealing with bi-directional traffic, the detection of multiple pedestrians, Automatic Emergency Braking for trucks and Adaptive Cruise Control (ACC) on highways.

According to Yole Research, the global automotive radar market will reach $8.6 billion in 2025, which represents a Compound Annual Growth Rate (CAGR) of around 16% between 2015 and 2025.

Moshe Meyassed, CEO of RFISee, said: "Today's automotive radars typically provide low resolution and limited detection range. Our ability to combine long range, high resolution and superior accuracy can be the key for the high-quality sensor fusion between the camera and the radar that the automotive industry is looking for.

"The sensor fusion that RFISee is introducing will open new frontiers for adding effective AI layers to the fused radar and the camera data. As a result, car manufacturers and drivers alike will benefit from crucial improvements in safety and accident prevention, effective operation in low visibility and increased automation in vehicles."

Accessing IT talent

IN ORDER TO SUSTAIN AND GROW THE UK'S TECHNOLOGY SECTOR WE NEED A SIMPLE AND AFFORDABLE IMMIGRATION SYSTEM, AS **DAVID HAROLD** EXPLAINS TO NEW ELECTRONICS

The shortage of Science Technology Engineering and Mathematics (STEM) skills in the UK is a real concern. You've no doubt heard that many times, and now over several years. But the timing is NOW to act on it. Why? If the UK is to maintain and grow these industries in the wake of Brexit and COVID-19, it must have reliable access to talent from overseas.

Research, by EDF Energy, forecasts that STEM jobs will grow at double the rate of other occupations, creating 142,000 jobs by 2023. While research by STEM Learning in 2018 highlighted a shortfall of 173,000 skilled workers in the UK, with 89% of STEM businesses struggling to recruit at a cost of £1.5 billion a year.

"At Imagination we have struggled to find engineers in the UK, and therefore have had to look outside of the UK for talent."
David Harold

People have become more risk averse when it comes to taking jobs overseas and data analysed by the BBC last year concluded that UK jobs were attracting less interest from other European workers - we must make sure that the UK remains an attractive destination, so our immigration policies will be crucial.

At Imagination we have always struggled to find enough engineers in the UK, although we do prioritise the UK for searches, and therefore have had to look outside of the UK for talent. Historically, they have come eagerly but there is a worry that things are changing and that there will be significantly more hurdles to jump and barriers to cross, and that ultimately our tech industry will suffer.

What needs to happen to ensure we can access talent from abroad?

Recent changes to the immigration shortage lists are very much welcomed when it comes to expanding critical roles. At Imagination we've been able to hire for roles such as research and customer engineers more easily. However, it's not enough and more needs to happen. Looking to the immediate future, three issues need to be addressed: the complexity of the immigration process, the costs of visas and the ability to switch visas.

Sourcing talent

When sourcing talent from outside the UK, it needs to be as easy and straight-forward as possible for the candidate. The effort, time, financial cost and emotional investment required by someone to relocate to the UK is huge – often starting in a new role in a new company is daunting enough but add to that the pressure of moving your family and being in a new country. Going through all the necessary red tape adds to this effort, even more so if doing visas for your family.

The more the process can be simplified with clearer guidance, the less risky the move will be perceived by the candidate.

The cost of visas needs to fall significantly, especially for families. While it is not surprising that there is a cost involved, the average family is looking at over £10,000 to relocate to the UK and in short someone must pay it. Typically, the costs are absorbed by the candidate, the company or both. From a company perspective, it needs to both support the candidate and family but also protect its investment so clawback policies are commonplace.

The problem with large sums like this is that it feels like a debt or loan. And this is where we come back to effort and risk, and whether it is worth it to the candidate. For smaller companies that need to be more risk averse with such a large sum of money, this can be a really tough decision and often result in a prolonged struggle for talent that is not only financially costly but can also impact productivity, growth and culture.

We understand a need for the cost, but it needs to be significantly reduced with solutions for families put in place. For example, the government could lower the costs of visa extensions to candidates that are keen to stay in the UK following their initial visa duration or make children's visas free to encourage families to relocate and commit to the UK long term.

Finally, we need to make it possible for people to switch visas from within the UK as currently this is not possible. The UK needs to open the sponsored visa process to all visas because it helps retain the talent UK tech companies have already invested in while encouraging their partners on dependant visas to take up higher skilled work and contribute into the UK economy.

Imagination is made up of people from over 40 different nationalities and we believe that gives us a competitive edge.

As a business we hope that the UK can encourage more children and young adults into STEM and recognise the challenging and fulfilling careers, but we also need to continue to access talent from around the world. That can only happen if we keep the immigration process simple and affordable.

•David Harold, Chief Marketing Officer, Imagination Technology

A revolution in **military affairs**

With the rise of AI and machine learning are we prepared for a new type of warfare? By **Neil Tyler**

From the advent of the Dreadnought battleship back in 1906 to the rise of nuclear weapons during the Cold War, militaries around the world have often talked about a 'revolution' occurring in military affairs but in truth, while the technology changed, the way in which wars were fought did not - whether that was in Korea, Vietnam, The Falklands or Iraq.

Today, however, there is a growing belief that over the next 20 years, or so, we will experience a revolution in warfare, with significantly more changes than we've seen at any time in the past 50 years – from weapons' capabilities to the way in which wars are conducted.

Revolutionary technologies from new sensors and embedded computers to drones and robotics, together with developments in artificial intelligence and the use of big data, are being combined and will radically change the nature of warfare.

In terms of the future battlefield we could see swarms of robotic systems, both as sensors and weapons, the deployment of laser weapons, reusable rockets, hypersonic missiles and unmanned, autonomous vehicles.

The Ministry of Defence (MOD) in the UK is, for example, developing a state-of-the-art weapons system, known as Directed Energy Weapons (DEW), which operates without ammunition.

These laser weapons systems deploy high energy light beams to target and destroy enemy drones and missiles and are expected to be trialled in 2023 on Royal Navy ships and Army vehicles but, once developed, could be operated by all three services.

Part of the MOD's "Novel Weapons Programme" which is responsible for the trial and implementation of innovative weapons systems, the MOD has commissioned three Dragonfire demonstrators that will combine multiple laser beams to produce a weapons system.

Whatever the weapons programme being developed, however, underlying all these new technologies is the growing international competition that is being seen between the likes of the US, China and, to a lesser extent, Russia.

"The marriage of rapid technological progress with strategic dynamism and hegemonic change could prove especially potent," argues Michael O'Hanlon, a senior fellow and director of research at the Brookings Institute.

"The return of great-power competition during an era of rapid progress in science and technology could reward innovators, and expose vulnerabilities, much more than has been the case to date." Michael O'Hanlon

"The return of great-power competition during an era of rapid progress in science and technology could reward innovators, and expose vulnerabilities, much more than has been the case to date," he suggests.

According to O'Hanlon 'revolutionary' change is likely and we'll see significant developments across all forms of technology from communications to projectiles, forms of propulsion and platforms.

The biggest revolution, however, is likely to come in terms of the use of AI, big data and the use of autonomous systems.

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When it comes to autonomous systems leading defence contractors, Boeing and Northrop Grumman, are already building unmanned fighter jets. With no need for crew facilities, these drones will be able to provide the military with more capabilities both in terms of payload and longer range. It's thought that Lockheed Martin's F-35, which is now entering service both in the US and around the world, could quite possibly be the last manned strike aircraft that most countries will look to buy.

If that proves to be correct then drones look set to dominate the skies by 2050.

Above: In 1906 HMS Dreadnaught revolutionised naval warfare

Ethical issues

Today, we talk a lot about 'a new normal' and in the future, when it comes to defence, unmanned and autonomous systems will become every-day devices that will be deployed in all manner of situations.

But the use of autonomous vehicles and drones raises some interesting ethical issues.

How independent should drones become, will decisions to engage with an enemy still be made by "a man in the loop", or will those decisions be made by the robots themselves?

In an attempt to address this, there is growing interest and work in the development of 'ethics' software that will be capable of querying decisions or determining whether the use of a specific weapon, in a particular situation, might violate the norms of a 'just war'. The goal of such software is to aid, not replace, human decision-making.

Speaking at COGX, earlier this year, Dr Ozlem Ulgen, an international lawyer specialising in autonomous weapons, explained that there was a long tradition of setting rules around forms of conflict.

"Regulating warfare, setting boundaries and establishing ethical underpinnings for warfare have a long tradition when it comes to warfare and by establishing such rules we regulate warfare and legitimise it.

"There are basic principles governing military engagement and the conduct of hostilities - combatants need to be mindful of situations, limit harm and show awareness. So the development of AI and machine learning and their use in warfare raises real and interesting challenges."

The potential to use AI combined with autonomous machines on the battlefield is enormous.

According to many AI is 'very much' the future, but questions are being asked as to whether AI can, no matter how clever, replace humans.

"Technology can only enhance and help humans by working alongside them," argues Dr Vitor Jesus, Senior Lecturer in the School of Computing at Birmingham City University.

"I'm sceptical about the use of AI. When you look at its use in cyber security it tends to create more problems than solutions. While AI is a great tool when used to help humans, it is rather poor when deployed to replace them."

"Hosting complex systems is a challenge and we know that when it comes to cyber security, complexity can see systems compromised."
Dr Vitor Jesus

Below: Could the F-35 be the last manned strike aircraft?

Dr Jesus makes the point that while technology will certainly evolve, "I don't believe that we will see the kind of breakthrough in technology that will be required in the next 5-10 years. I don't think that AI techniques and the models and maths behind them, will improve sufficiently.

"AI is great when it is used to help us better understand what we know well, patterns and images, for example - it does a good job. The problem comes when something isn't found in 'the catalogue', i.e. a Black Swan event. We need a new way of thinking about machines and reasoning."

He also makes the point that the growing complexity of systems brings additional problems.

"Hosting complex systems is a challenge and we know that when it comes to cyber security, complexity can see systems compromised."

AI is designed to learn in operation, and a service attack could result in turning a system against its owner, to the benefit of the adversary, suggests Dr Jesus.

"Basically, you'll have created an insider working within the system. Can we use AI to increase safety and reliability? Not yet. My simple message would be 'don't do it'. AI works as an advisor, but should not be allowed to make the final decision - a human needs to be responsible for that."

Despite his concerns defence systems designed to counter missiles already rely on robots to defend assets, such as warships. Their ability to react to a fast moving threat – a missile – is now well beyond the capabilities of humans.

Both China and Russia are believed to be designing software that will remove the human from some decisions, so responsibility for actions, responses and ultimately deaths is destined to become "very,

very, very diluted", according to Emmanuel Go , a French air-force expert on robotic warfare, "and you can't pin war crimes on a robot."

Robots and the use of autonomous systems raise a number of additional questions – could their use mean that adversaries are more inclined to strike at civilian targets, if they are unable to engage and take out military adversaries? Could they encourage countries to turn more quickly to military solutions and start more wars?

Technologies combined

According to Dr Bryan Wells, NATO's Chief Scientist, "Rarely does an individual technology make the difference, it is when they're combined. For NATO the key characteristics determining the future of technology in this space are: distributed, digital, interconnectedness, and intelligence, and we judge that AI, ML and autonomy will be the key areas we should be looking at over the next 5-10 years – looking beyond that, we see biotechnology and quantum coming to maturity.

"The pace of technology is accelerating but so too is the breadth of technology, which will give rise to greater choice for leaders who will be confronted with moral and ethical issues," he said.

The launch of the HMS Dreadnought, an all-gun battleship by the Royal Navy, back in 1906 revolutionised naval warfare. It made all existing vessels obsolete and risked Britain's then naval dominance – likewise with today's new technologies, can the West\NATO retain its lead in military robotics in the face of competition from the likes of China and Russia?

In the UK, our emerging capabilities in terms of AI could benefit by adopting current and near-term quantum technologies, according to a recent research paper published by the Defence Science and Technology Laboratory (Dstl), on behalf of the MOD.

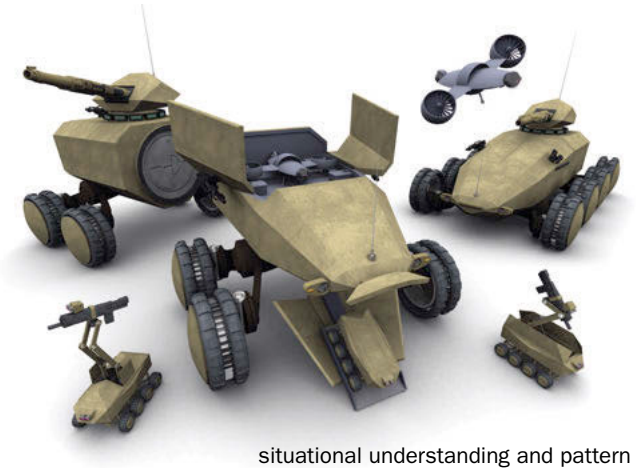
According to the report, by embracing quantum technology the UK could see the pace, precision and pre-emption of decision making enhanced for military commanders.

Dstl's report identified commercially available quantum computers – 'annealers' – that could have the potential to run an important and versatile class of AI software at speeds vastly in excess of normal digital computers. This software is based on pattern-matching, which imposes extremely high loads on classical digital computer architectures - the unique properties of a quantum annealer, means that it can execute a neural net in one machine cycle instead of thousands or millions.

According to the report, quantum neural nets could be used to perform Quantum Information Processing (QIP) to search archive, near real and real-time data feeds, automatically looking for features of interest, detecting anomalies and instances of change.

This would significantly improve the time, cost and quantity of military data processing.

Over the next 5-10 years, within the MOD and more widely, QIP technologies look set to be applied to control systems in aircraft, missiles, fire control and defensive systems, sensor data processing such as data fusion, navigation, resolving signals in noise, interference and jamming, AI situational understanding and pattern analysis.



Above: A computer graphic simulation of the Future Protected Vehicle

"Our ability to harness the capabilities of science and technology will be fundamental and directly linked to our ability to deliver defence and security." Gary Aitkenhead

Below: Computer generated image illustrating the use of DEW on a Wildcat helicopter

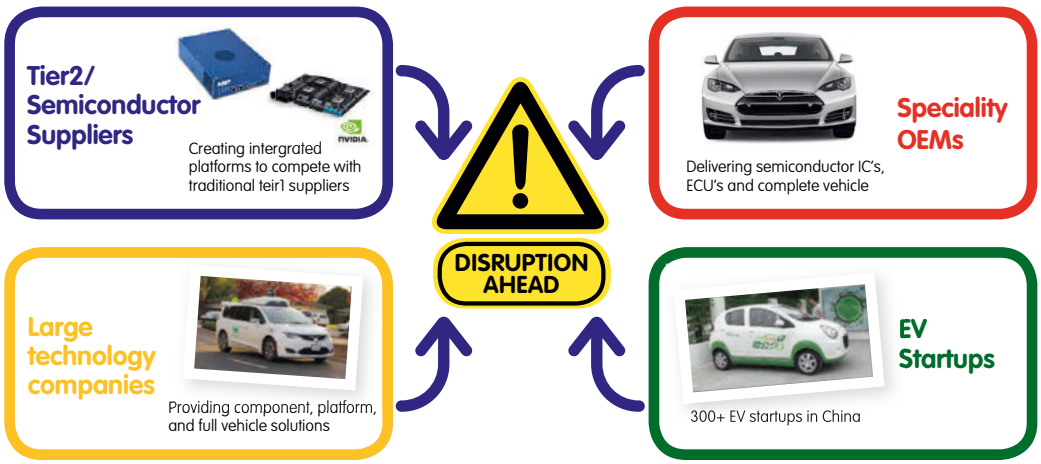
Commenting Gary Aitkenhead, Dstl Chief Executive, said, "Quantum technology is a game-changer for defence and society - one that maintains the security of the UK, and offers significant economic benefits."

"The pace of change over the past 10-15 years has been rapid and the threat landscape too, has changed markedly," added Aitkenhead. "Our ability to harness the capabilities of science and technology will be fundamental and directly linked to our ability to deliver defence and security."

Many countries are now upgrading their defence platforms after the decades of asymmetric warfare in the Middle East, and their investment in new platforms is looking to incorporate AI and other tools that turn data into tactical information.

Investment in digital technology is accelerating and the focus is on developing new platforms and systems that are faster and more agile and, as a result, this technology-focused approach is seeing the world's militaries increasingly having to engage with the commercial sector in order to identify technological innovation.

While some areas of military technology may not change dramatically in the coming years, whatever the technology and the science behind it, the key is likely to be how these individual technology trends interact with one another, and what innovations will arise in terms of how they are employed on the battlefield.



A SUPPLY CHAIN IN FLUX

How will tier-1 suppliers weather a changing automotive ecosystem. By **Richard Pugh**

In the coming years, Tier 1 automotive suppliers have an enormous opportunity with the development of autonomous vehicles (AVs) but there are challenges - the whole supply chain is being disrupted by new participants and new technologies.

Semiconductor companies and specialist OEMs are now major players and newcomers include both well-established companies and small start-ups.

This will affect the role of tier 1 suppliers, and they will need to adapt to ensure that they continue to add solid value to the supply chain. One important step in that direction is the adoption of new system verification strategies as a response to the increased difficulties posed by vehicles that have to be safe enough to drive themselves.

With AVs the architecture is moving from one containing many small, independent engine control units (ECUs) to a more centralised approach with higher-powered multicore processors running extensive suites of software. This brings new players into the picture, and means that the supplier ecosystem must be reinvented to reflect these new contributions.

Tier 1 suppliers, in particular, will encounter a number of specific new challenges: large technology companies like Google, Amazon, and Baidu may weaken the traditional supply chain by doing things differently; OEMs may work directly with tier 2 semiconductor companies, squeezing out the tier 1 supplier; electric-vehicle start-ups, especially in China, are opening up new markets and may bypass tier 1 suppliers in the process; and some specialist OEMs, like Tesla, are integrating vertically, leaving out the entire traditional supply chain.

This changing environment is forcing all players to rethink their roles in the supply chain. Sticking to old models will decidedly not be a winning strategy. In order to understand where changes and new opportunities lie, we need to understand the implications of this new electronic push within vehicles.

Figure 1: The entire supply chain is being disrupted by new players and new technologies

Silicon content is booming

Increased electronics sees more silicon in an autonomous vehicle, and this poses a unique challenge to tier 1 systems designers. There is specific growth in the use of systems-on-chip, or SoCs that are sophisticated, highly integrated chips that include custom computing capability. No SoC can be complete without considering the software that the SoC will execute and this adds a new dimension to silicon verification.

Traditional automotive flows use four different tools for verification. New flows are adding a fifth.

Those traditional flows include:

- Virtual prototypes that leverage high-level models of hardware behaviour. While these models execute quickly, their accuracy is insufficient for full verification.
- Hardware-in-the-loop (HIL) is an option once hardware is available and stable. Because this relies on existing hardware rather than a fully instrumented verification testbench, stimulus tends to be non-deterministic, and, when things go wrong, debugging is difficult.
- Software simulation provides full cycle accuracy and has excellent debug capabilities, but it runs far too slowly for full verification coverage of both hardware and software in an SoC or a system-of-systems. Testing software may mean first booting an operating system before testing how drivers interact both with the silicon and that operating system and involves millions of cycles of execution.
- Hardware prototyping options lack the capacity, debug visibility, and

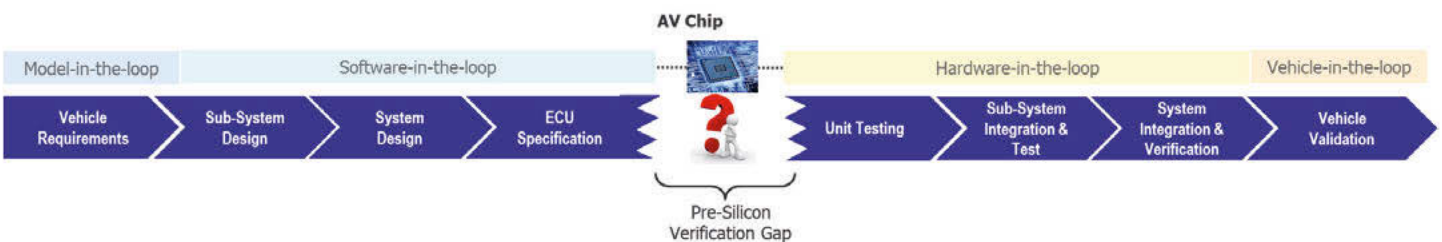


Figure 2: Critical to success in the automotive realm is full verification that must be completed before chips are produced

Source: Mentor, a Siemens Business

Figure 3: Emulation can model all electronic content and coordinate it with a full set of mechanical models, the only way to manage such a large computing task to meet a project deadline.

design-change turnaround time necessary for full-chip and system-of-systems verification.

New on the scene are digital-twin representations of vehicles, modelling not just the silicon, but all aspects of a vehicle. These represent an increasingly important component of vehicle verification and validation strategies and represent a significant computing challenge.

Given the amount of heavy lifting that silicon will perform in vehicles and the enormous cost of having to redo a silicon chip, full verification must be completed before chips are produced, creating a pre-silicon verification gap. Bridging that gap is critical - verification must include not just the silicon in isolation, but the ways in which the silicon interacts with the rest of the vehicle.

PAVE360 and Veloce

Siemens' PAVE360 programme was created for automotive design. Playing a central role is the Veloce emulation platform for verification and validation of automotive electronics and subsystems – an emulator is a special-purpose supercomputer that models integrated circuits before they're built.

Because it uses hardware instead of software to do the modelling, it can run 100-10,000 times faster than software simulation can and it's a full-on computing environment dedicated to simplifying specific verification tasks.

While new to automotive electronics, emulators have long proved their worth in verifying complex SoCs for the telecommunications, storage, and mobile markets.

Emulation is the only way to thoroughly verify an SoC and as SoCs move into vehicles, emulation becomes a necessary automotive verification tool.

It allows connection to virtualised data sources to be used as test stimulus. By virtualising these sources rather than relying on real-world sources, the test data is deterministic and repeatable, speeding up debug and resolution of any issues found during verification.

Full verification involves more than just exercising functionality. It's important to confirm that power doesn't exceed its budget.

Safety must be verified and documented in accordance with the ISO 26262 safety standard. Silicon chips have internal test infrastructure (design-for-test, or DFT), and those circuits must be verified. All of these tests contribute to the overall verification coverage – that must be tracked and reported.

These are the specific tasks performed by the software applications that run on Veloce emulators. Those applications abstract the implementation specifics of the tests, allowing verification engineers to work at a higher level with greater productivity.

Emulators also provide a way to verify that those SoCs and other chips correctly interact with the mechanical components they control. Those components rely on tools and methodologies different from those used in silicon design.

PAVE360 brings these tools together using standard electronic and automotive interfaces like transaction-level modelling (TLM), part of the IEEE SystemC standard used by the Vista verification tools, and the functional mock-up interface (FMI), used for interactions between electronic and mechanical tools.

Finally, digital twins require maintenance of a digital model of a system in synch with a real version. That means modelling all of the electronic content and coordinating that with a full set of mechanical models. Emulators are the only means of handling such a large computing task in a meaningful timeframe.

Verification of new automotive designs has become much more complex due to the integration of electronics and mechanical components. As electronics pervade autonomous vehicles, silicon must be verified in conjunction with all of the non-electronic parts of the vehicle. SoCs must have both their hardware and their software thoroughly vetted. And digital twins must be built and exercised. Early pre-silicon verification means that the first chips built will be correct, avoiding lengthy and expensive re-spins.

Tier 1 companies belong at the centre of this verification effort, pulling together all of the components and subsystems into one coherent model. It's a job that's easy to get wrong without the right tools, and yet, done right, it lets tier 1 suppliers add value and differentiate.

There's no practical way to achieve this without PAVE360 and emulation. By adopting this new-to-automotive methodology, tier 1 suppliers reinforce their value in the supply chain, partnering across the ecosystem as well as up and down the value chain.

By adapting to these new realities tier 1s can ensure they remain a critical, valued part of the automotive supply chain.

Author details: Richard Pugh is a Product Marketing Manager in the Emulation Division at Mentor, a Siemens business

A 'CAPITAL' IDEA

Siemens has extended its Xcelerator portfolio to help transform electrical/electronic systems development, as **Neil Tyler** discovers

Back in June, Siemens Digital Industries Software announced that it was expanding its Capital electrical/electronic (E/E) systems development software portfolio.

As Nick Smith, Business Development Director, Integrated Electrical Systems, explained, "The move is intended to build on Capital's existing capabilities for design, manufacture and service of electrical systems, and the portfolio will now encompass E/E system and software architectures, network communications and embedded software development."

Capital forms part of the company's Xcelerator portfolio of software, services and its application development platform.

The announcement has come in response to the huge growth in the complexity associated with modern E/E systems, which require integrated electrical, electronic and software systems to support and drive further innovation. These new complex systems also require robust verification and traceability.

"The electronic intensity of products, from aircraft to complex medical scanners, is increasing rapidly," said Smith, "and the number of software lines of code and the number of network signals has been rising dramatically. In 2014 the industry was predicting 30 million lines of code in the average car by 2020, today it's actually 150 million and, with network signals, we've seen a similar rate of growth."

This growth comes at a time when many industries are working with outdated, disconnected and siloed product development methods, while those same industries are facing new, dynamic trends such as electrification, autonomy, increasing programme complexity and new compliance requirements.

"The need to deliver coherent solutions to help meet demanding productivity and safety demands has never been greater," according to Smith. "The inability to collaborate, due to working in silos, has meant missed and misinterpreted requirements, a document heavy process, poor data flow and cumbersome change management. Industries are wasting millions in investment due to operating in silos."

As an Electrical Integration Lead at a commercial aircraft company said, "With the increase in electrical systems content the validation task is so large that it can put the whole organisation at risk. This is why we must change."

With too many product development approaches siloed in organisations, the result is that not only is innovation and quality undermined, but issues with designs tend, typically, to be exposed only when multiple sub-systems are brought together during system integration, which can then cause program schedules to slip as a result of engineering changes.

The ability to create transparency between these silos and blur domain boundaries across the E/E systems lifecycle is vital.

By connecting the different development stages it's now possible to facilitate approaches that foster data sharing across the full product life cycle.

"There are plenty of opportunities to reduce errors and accelerate development," explained Smith. "Coping with complexity is what we are trying to address as well as breaking down the silos that currently exist."

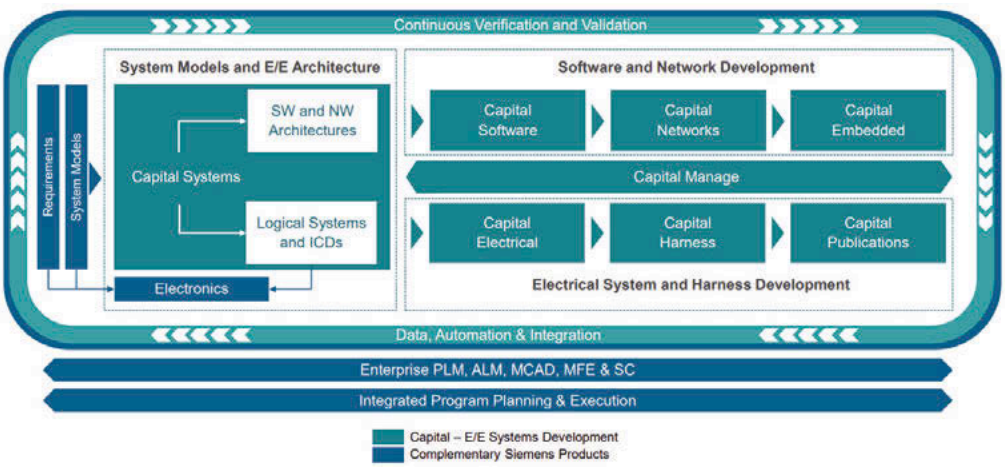
Capital expanded

In response, Siemens has unveiled extensions and integration of its Capital software suite for E/E systems and software design, with a major focus now being on embedded software and network communications.

Capital, which joined Siemens Digital Industries Software following the acquisition of Mentor Graphics, has now been integrated with other Siemens tools and platforms, such as Xcelerator.

Capital can support software architectures, communication networks and AUTOSAR compliant embedded software within the broader Xcelerator portfolio, helping to transform E/E systems development.

"Our aim is to reduce programme



Below: Capital E/E systems development enabled by Xcelerator

risks and blur the boundaries between the mechanical and electrical. These new capabilities will make it possible to design and assess E/E systems and enable support for integrated end-to-end model-based design, manufacturing and service domains," explained Hans-Juergen Mantsch, Technical Director Integrated Electrical Systems.

Capital has evolved over time and now delivers a holistic E/E systems development environment and, according to Smith, by adopting a model-based engineering paradigm, engineering processes will be able to increase automation and quality.

"Such automation is not limited within a specific domain but expands the connection between the different disciplines. As a result, companies can now promote and enable inter-dependencies across disciplines with respect for the downstream workflow requirements," said Smith.

The expansion of Siemens' Capital portfolio brings new levels of integration.

"Capital has been extended into a broad-based portfolio that will transform system design for complex products in markets such as automotive, aerospace and adjacent markets," said Mantsch.

Capital is integrated with the Teamcenter portfolio for product lifecycle management, NX software for mechanical design and Mendix low code development environments, creating a comprehensive E/E systems development solution.

As mentioned earlier, modern E/E systems are characterised by huge levels of complexity and interconnectedness, so in order to effectively manage these interconnected challenges, the E/E systems development solution from Capital now encompasses E/E systems architecture, electrical systems, communication networks and embedded software.

Its support of integrated end-to-end model-based design, manufacturing and service domains looks set to transform quality and reduce costs.

"Capital's integration with Siemens' model-based systems engineering (MBSE), MCAD, product lifecycle management (PLM), simulation and manufacturing solutions will help enable a comprehensive digital twin of the whole product," according to Mantsch, "and these integrations deliver requirements management, multi-domain functional modelling, software simulation, application lifecycle management and manufacturing plant simulation."

Siemens has sought to bring together formerly siloed disciplines required to develop and support smart, connected products and by integrating Capital with existing platforms, it is enabling a system-wide view of products which will enable customers to economically achieve the performance and quality that's required.

"The electronic intensity of products, from aircraft to complex medical scanners, is increasing rapidly," Nick Smith

The end-to-end capture and definition of the E/E system functionality enables the creation of a comprehensive digital twin for early simulation and verification which can now take place sooner in the product development process, reducing time to market.

The model-based approach of Capital will help enable high levels of automation and data continuity via a digital thread connecting product optimisation, realization and certification.

But as well as supporting an end-to-end flow, Capital is also flexible and can adapt to specific customer needs, supporting individual ways of working while providing support for necessary industry standards as part of an open ecosystem.

The announcement by Siemens is an important one as it delivers a new set of capabilities for customers who are creating complex system products, and drives system development and digital model-based systems from architecture, into design, development, manufacturing and services.

TECHNOLOGY TO THE RESCUE

Finding malicious flows hidden in the traffic of millions of connected devices is a huge challenge, but a solution is at hand.

By **Claire Huckerby-Brown** and **Richard Parks**

Network metadata provides an overview of what is happening on a network without storing the entire payload, thus providing an effective, lossy compression. Along with timestamps and the amount of data transferred, this covers a lot of information; from IP source and destination addresses, to ports and protocol, right through to Secure Sockets Layer (SSL) certificates, Domain Name System (DNS) request/responses and HyperText Transfer Protocol (HTTP) host names.

A carrier scale network operator may be interested in a particular flow for a variety of reasons – for example, it may be malicious, and part of a cyber-attack.

What is vital is that metadata is extracted from every single packet; this is referred to as un-sampled traffic monitoring and the task is compounded by the fact that there is no single data pipe for the internet. There are literally billions of ingress and egress points, with routes that can be used by flows to get from an ingress to an egress. Furthermore, while there are typically several 'cores' to a carrier's network, we now have edge computing, edge datacentres, cloud and mobile broadband in 3G, 4G and 5G, too.

Data rates are increasing exponentially, rising from 100GB per day in 1992 to a projected 150,700 GB per second in 2022. This means that there is continually more data to monitor between a growing number of devices. These figures highlight the need for higher rate network monitoring.

Data inspection

At full line rate, 4x100G Ethernet connections (as opposed to 1x400Gbps, which is a single network interface with a bandwidth of 400Gbps) can ingress up to 560 million packets per second. To give complete visibility, un-sampled traffic must be processed in real time; this is particularly important from a forensic evidence point of view.

Trying to find a single malicious flow amongst other malicious flows in 4x100GbE traffic can be like trying to find a needle in a haystack, with a box of other needles thrown in for good measure.

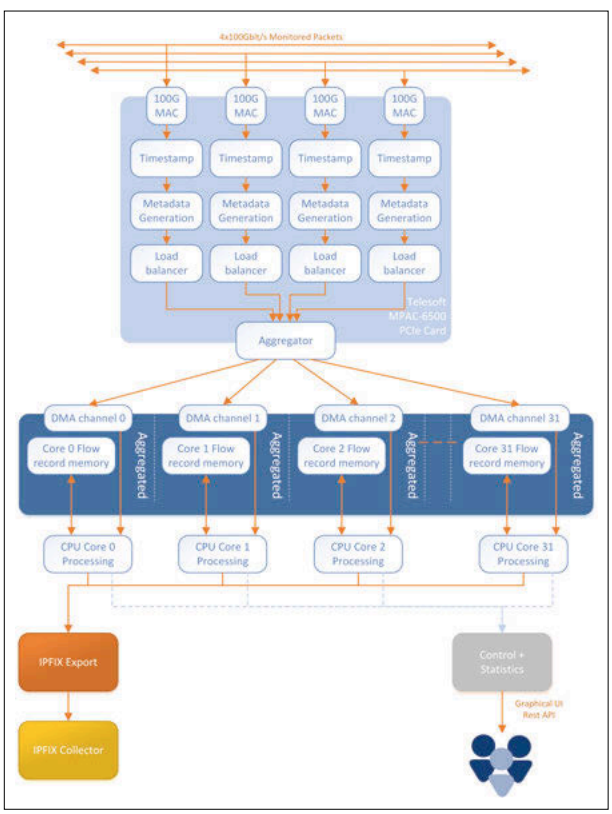
There are many software-based metadata extraction solutions available that can be installed on any commodity hardware, but this means they are also inherently rate limited by that commodity hardware. Typically, this would be several Gbps, or at a stretch 10Gbps.

Extracting network metadata at 4x100Gbps requires very high-speed processing, typically this can only be achieved using dedicated hardware, such as a Field Programmable Gate Array (FPGA) or an Application-Specific Integrated Circuit (ASIC). Both are used to accelerate calculations or processing and can remove system bottlenecks when used with processors, increasing the overall performance.

Faster results

Telesoft has shipped 100G Flow Probes since 2016 and has continued to increase the throughput and features ever since. Its 4x100GbE Flow Probe monitors

Figure 1: Global device and connections (Source: Cisco VNI, 2018)



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networks in real time, generates un-sampled flows and is completely passive.

At the heart of the system is an Intel Stratix 10 FPGA, which receives the 4x100Gbps of network traffic and performs metadata extraction. The metadata is then passed to multiple processing threads where the packet metadata is combined into flows. Finally, the flows are enriched with additional information.

Packets are de-tunnelled in real time; if tunnelling is present then it is automatically detected, and the encapsulated traffic exposed. For complete visibility, in this case, the metadata for both the outer tunnelling protocol, and the encapsulated traffic within, is extracted.

The metadata extraction is feature-rich and extracts data from all layers of the Transmission Control Protocol (TCP)/IP model, right up to and including the application layer where HTTP request method, host, target and the status code are all sent up to the host. Furthermore, DNS packets are identified and forwarded on for the host to extract DNS flags, type and the domain name.

The Stratix 10 has been designed to meet the high-performance demands of high-throughput systems, such as Telesoft's 4x100GbE Flow Probe, with transceiver support up to 28.3Gbps for chip-module, chip-to-chip and backplane applications; as well as up to 10 TFLOPS of floating-point performance. To enable high-speed host data processing, the metadata is delivered to the host over multiple Direct Memory Access (DMA) queues. Each queue is independently serviced by a dedicated host thread. The FPGA performs bi-directional flow-safe load balancing across the DMA queues, thus ensuring that all packets associated with any given uni-directional or bi-directional flow are delivered to the same host processing threads.

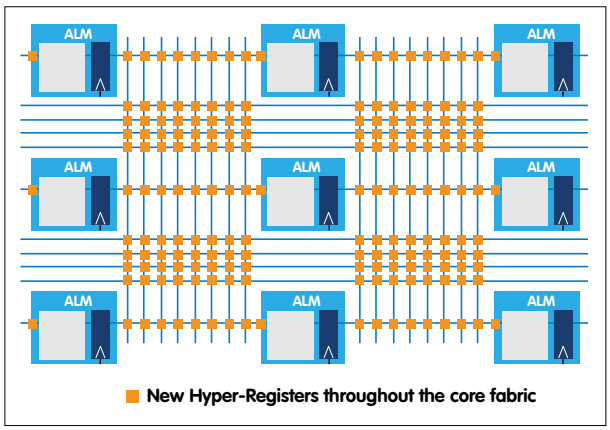


Figure 2: Block diagram of the Telesoft 4x100GbE Flow Probe

The host performs additional processing of the packet metadata to enrich the flow records with additional metadata. As an example, the host can perform a lookup of IPv4 / IPv6 address ranges against a live programmed tree of Classless Inter-Domain Routings (CIDRs) that provide Geo-Location, AS and IP reputation metadata. As each of these factors have temporal sensitivity it is essential that these matches are performed at the point of ingest.

The Stratix 10 GX devices are built on Intel's 14nm tri-gate process and have a tiled architecture such that the chip itself is comprised of several smaller chips, or tiles. The logic is on one, monolithic die, while the transceivers are on separate tiles in groups of 24 channels; this architecture results in the highest transceiver count of any FPGA (with 144 full duplex channels). Intel has different varieties of transceiver tiles, some of which, alongside the transceiver channels themselves, have PCIe Gen3 x16 hard IP, as well as some with 100G Ethernet MAC hard IP – both of which are used by Telesoft in its flow probe.

Hardened IP enables developers to use these interfaces without worrying about whether they will meet performance requirements. In addition, there is no need to use FPGA logic in the device to implement these IP blocks, meaning it can be used for other features. The tiled architecture is made possible by the use of Intel's innovative Embedded Multi-Die Interconnect Bridge (EMIB) packaging technology.

The differentiating factor

Stratix 10 GX devices feature Intel's Hyperflex architecture, which introduces additional, bypassable, registers throughout the FPGA fabric. These registers, called Hyper-Registers, exist on every interconnect routing segment and at the inputs of all functional blocks (logic blocks, memory blocks and DSP blocks); they are also distinct from the conventional registers that are contained within the Adaptive Logic Modules (ALM).

These Hyper-Registers mean an FPGA designer can retime registers to eliminate critical paths, adding pipeline registers to remove routing delays. This approach also means that all of the FPGA's logic resources are available for logic functions, instead of being sacrificed as feed-through cells in conventional architectures. The design tools can select the optimal register location automatically as well as reducing routing congestion.

Conclusion

Networks are complex environments, where speed and performance are measured in the smallest fractions of a second. The threat presented by a connected world relies, to some extent, on hiding in plain sight, due to the deluge of data that enters into, flows through and exits the many millions of networks found around the globe.

Metadata is a crucial tool in combating this threat, and flow probes are the practical implementation of that tool. Through the performance offered by integrated solutions like the Intel Stratix 10 GX FPGA, and Telesoft's ingenuity, networks are safer for all users.

Author details: Richard Parks is FPGA Team Leader at Telesoft and Claire Huckerby-Brown is a Field Applications Engineer at Intel

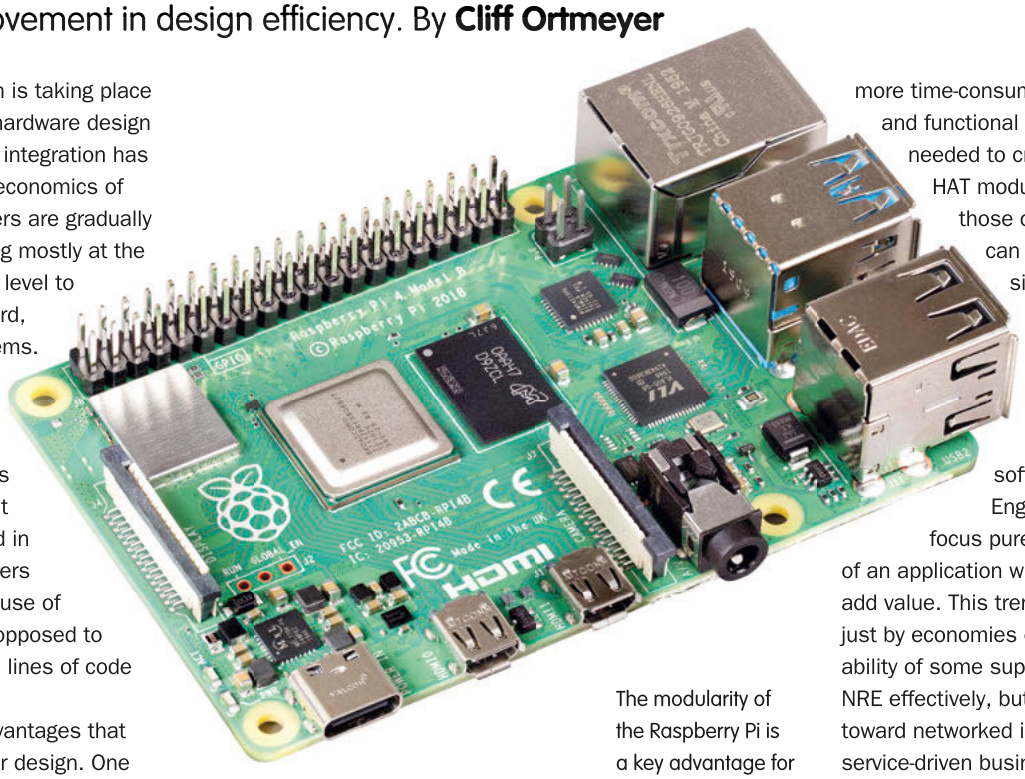
A **MODULAR** REVOLUTION

A quiet revolution is taking place in hardware design, causing a dramatic improvement in design efficiency. By **Cliff Ortmeyer**

A quiet revolution is taking place in electronics hardware design and, as silicon integration has continued (fed by the economics of Moore's Law), engineers are gradually moving from developing mostly at the component and circuit level to working more with board, modules and subsystems. The benefit has been a dramatic improvement in the efficiency of electronics design. It is a shift that is now being replicated in software, with developers looking to make more use of reusable modules as opposed to relying primarily on the lines of code they write themselves.

There are many advantages that lie in a shift to modular design. One is greater ability to share in the economies of scale that come from the use of platforms that attract many customers. Industrial users have a long experience with modular hardware. The Versa Module Eurocard (VME) and CompactPCI standards provided integrators and Original Equipment Manufacturers (OEMs) working in low-volume markets with the ability to use high-performance computing. They could perform more extensive customisation of a computer's capabilities without having to invest time and effort in high-end printed circuit board (PCB) design. Since those days, Moore's Law has delivered incredible gains in functionality while also reducing the cost of individual parts. The Raspberry Pi single board computer is a key example.

By leveraging the economies of scale that come with a smartphone System on a Chip (SoC) platform, the consortium behind Raspberry Pi has been able to deliver a far more effective product than would have been possible with a design created originally for educational use. The non-recurrent engineering (NRE) costs incurred by the silicon provider were easily absorbed by the primary target market, delivering much greater value to Raspberry Pi's target users. This cost advantage was passed onto the industrial sector. Integrators and OEMs have taken advantage of modularity of the Raspberry Pi platform, using the HAT expansion bus to add their own custom interface modules.

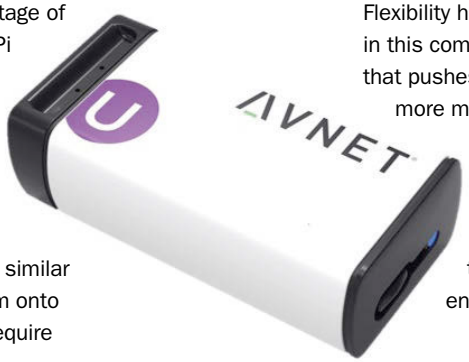


The modularity of the Raspberry Pi is a key advantage for design engineers

The use of the Pi modules frees engineering teams from having to source similar components and design them onto custom PCBs. These often require more time-consuming signal-integrity and functional checks than those needed to create the front-end HAT modules. Very often, those custom modules can use relatively simple two- or four-layer PCBs.

Software modules

A similar trend to modularise software has emerged. Engineers can now focus purely on elements of an application where they can add value. This trend is driven not just by economies of scale and the ability of some suppliers to amortise NRE effectively, but the larger trend toward networked integration and service-driven business models. An embedded system is often not complete today unless it forms part of a larger system of systems, such as the Internet of Things (IoT). In this environment, a device may be used to help deliver one or more services – many of which will be changed during the lifetime of the hardware used to support them. This combination of the IoT and the cloud is yielding new business models that leverage these capabilities, such as software as a service (SaaS) and pay per use. Flexibility has become a key criterion in this commercial environment: one that pushes implementors to seek more modular structures.



Modularity begins with the operating system. The operating system supports abstractions that are vital to building flexible, modular environments. Typically,

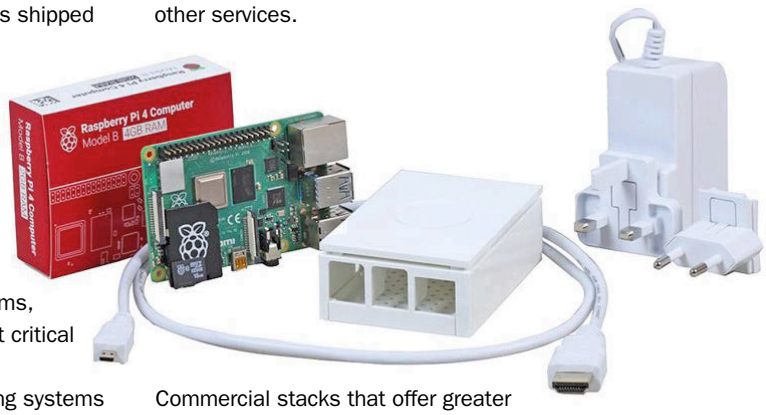
an operating system provides a set of services that range from simple input/output to full networking stacks, all accessed through a set of documented application-programming interfaces (APIs). As long as the services continue to support the APIs, the code that delivers them can change without affecting the applications that use those APIs. It is as true for the simple real-time scheduler FreeRTOS that is shipped with many microcontroller development tools as it is for commercial and more complex RTOS implementations, such as Wind River's VxWorks . VxWorks sets the industry standard for embedded operating systems, powering some of the most critical infrastructure and devices.

Linux and other operating systems can make memory management go further by making it possible to isolate tasks from each other. One possible issue with simple RTOS structures is that they operate in a completely unpartitioned memory space. Bugs or malicious behaviour in one task can lead to data and code being overwritten accidentally in another, leading to a system crash or other undesired outcomes. Linux uses virtual addressing, mediated by a hardware memory-management unit, to prevent tasks from accessing each other's memory spaces. They can only interact through operating system APIs or inter-application protocols built on top of these APIs.

Virtual memory addressing is not an absolute requirement for task isolation. Some microcontroller architectures, including several members of the Arm Cortex-M and Cortex-R families, can enforce memory protection in a flat memory space. Arm also provides the Trustzone secure software mode in a number of its processors, which make it possible to isolate sensitive software from user-level tasks. With this protection, it becomes easier to combine custom code with the growing range of off-the-shelf software modules that have been developed to cope with common tasks.

Integration of functions

Today, engineers have access to a range of free, open source software modules and protocol stacks available through Github, Sourceforge and other services.



Commercial stacks that offer greater support, additional functionality or certification for safety-critical applications are also on offer. The reference designs put together by silicon manufacturers will often combine a range of open source and proprietary functions to make it easier for customers to build prototypes through to full product implementations. In some cases, the reference design implements a full application that the end user can tune to their own needs.

Some system designers are taking advantage of the increasing modularity of software to construct development environments that tune parameters and generate code automatically. These tools often use block-based representations of software that the developer assembles on a graphical user interface. One example is Microchip's MPLAB Code Configurator for the PIC8, PIC16 and PIC32 microcontroller families.

Advanced applications, such as machine learning and image processing, are examples of areas where users can benefit from the high NRE investment of specialists and avoid the years of development time such software would require if users had to build it from scratch. Caffe, PyTorch and Google's Tensorflow make it possible to build, train and tune complex artificial intelligence (AI) models that easily integrate into embedded processing pipelines. For image processing, OpenCV is a widely used library that can easily be integrated into real-time applications. With the rise of machine learning, an increasingly common usage model today is for OpenCV to preprocess image data before being passed to an AI model built using Caffe or Tensorflow, with custom code being used primarily to provide the real-time response to events the model detects.

Bringing it all together

Developers now have access to cloud-oriented software modules and tools that easily integrate with common network stacks and RTOS implementations. This enables embedded systems of varying levels of complexity to be integrated into the IoT. Avnet's IoT Connect Platform, for example, provides cloud-based processing for complex tasks such as AI. As the system is defined by both cloud and embedded device software services, cloud providers such as Amazon Web Services and Microsoft Azure now provide a range of offerings that bring the two together: all leveraging the modularity of the software components they employ.

Modularisation is changing the required skillset of embedded software engineers. The balance of responsibilities is shifting from code development to an ability to construct flexible architectures based on pre-existing modules that allow for easy custom coding and runtime configuration as new services are deployed. By harnessing this modularity, OEMs and systems integrators can easily keep pace with the demands of customers that would simply be inconceivable by traditional means.

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What's all the hype about?

New processor ISAs appear rarely, so the RISC-V ISA has created a real 'buzz' among embedded engineers. **Mark Patrick** explains

New processor instruction set architectures (ISAs) really don't come along very often, so open-source RISC-V ISA developed within the University of California at Berkeley has created a real buzz in the embedded industry.

The RISC-V ISA was developed on the premise that any designer could use it to create processor cores and software compilers, and the project is now run by the RISC-V Foundation, with members that include a wide range of universities and multinational technology companies (Google, IBM, Microsoft, NVIDIA and Oracle, most notably), as well as chip makers and start-ups.

The aim of RISC-V was to learn from the mistakes of other processor ISAs. The key is stability – for the instruction set and the core – which is essential for encouraging as many engineers as possible to use such open-source technology across the ecosystem, making powerful processor cores much more accessible and usable.

Application developers can optimise their code for a frozen ISA with minimal memory footprint and power consumption, but still be scalable and compatible with future devices, allowing processor core developers to work on all kinds of different implementations of the instruction set.

These will have different latencies, sizes and power consumption, but will all have an underlying compatibility with each other, and with the tools encompassed within the ecosystem.

Providing this stability across the ecosystem was a critical part of the new instruction set. This was designed with 32-bit, 64-bit and 128-bit address spaces in mind, so compatibility across them can be maintained. The architecture is also designed with extensions, to provide the customisation that chip makers need for differentiation and for future application scenarios, but the ISA's foundations remain deliberately untouched.

The 128-bit ISA is still intentionally undefined, because as yet there is little practical experience with such large memory capacities in embedded systems. However, the fact that the architecture will support this larger address space highlights the forward-thinking approach taken. All of this means software written for, or ported to, RISC-V will run on all similar RISC-V cores forever, giving software managers a solid foundation that preserves their software investments.

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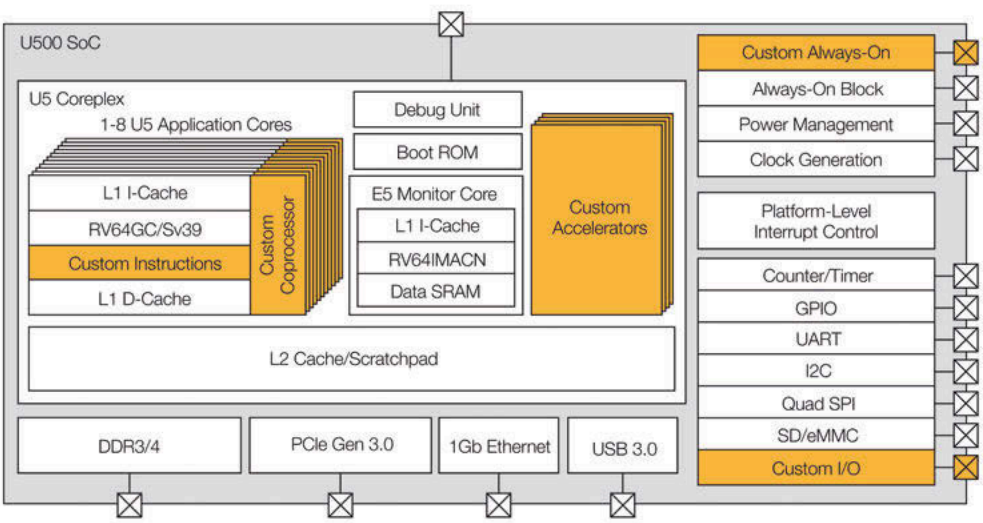


Figure 1: The U500 64-bit multicore open-source processor from SiFive

Processor cores

A wide range of processor cores are implementing the ISA, and a number of system-on-chip (SoC) devices are based around those cores.

Cores have been developed by Codasip, Syntacore, Hex Five and T-Head, while SiFive has pushed forward with a range of 32-bit and 64-bit SoCs.

SiFive launched its first RISC-V core in 2017 as a family of SoC platforms, adding support around the cores and chips. The devices are being built on a 28nm process for a 64-bit multicore Linux implementation, or on 180nm for the 32-bit low-cost IoT market with various peripherals.

The company's Freedom platforms comprise of a complete software specification, board support packages (BSPs) to bring up an operating system, development boards and base silicon, allowing customers to create their own silicon enhancements and customisations.

The Freedom U500 series is a fully Linux-capable embedded application processor with multicore RISC-V CPUs, running at a speed of 1.6GHz or higher with support for accelerators and cache coherency for machine learning, storage and networking. This supports standard high-speed peripherals including PCIe 3.0, USB 3.0, Gigabit Ethernet, and DDR3/DDR4.

The Freedom E300 series is designed as an embedded microcontroller for the IoT and

wearables markets. Based on the Freedom E310, the HiFive1 Arduino-compatible RISC-V development kit incorporates SiFive's E31 CPU Coreplex – a high-performance, 32-bit RV32IMAC core that is capable of running at over 320MHz.

SiFive has also used the RISC-V instruction set for the S2 core IP series, with a configurable core that can be as small as 13,500 gates (in the case of the RV32E 32-bit version). The S21 64-bit embedded core has separate instruction and data buses, along with two banks of tightly integrated memory (TIM). This enables SoCs to have an always-on low-power 32-bit CPU that can be combined with a high-end 64-bit CPU that switches on when applications demand elevated performance (such as in voice-activated smart devices).

Developments of this kind help address the growing need for connected devices with machine learning and IoT, where real-time workloads have generated a massive demand for greatly enhanced embedded intelligence at the edge.

The open-source nature of RISC-V has opened up SoC design to start-ups such as Kendryte, e-fabless and low RISC, but more mainstream chip vendors are also using the technology.

Microsemi has produced some development boards for SiFive, while NXP has its own RISC-V chip. Andes Technology and Greenwave have also developed ICs around the ISA. Faraday Technology has used the ISA for an ASIC platform for the design and mass production of next-generation edge AI and IoT SoCs. It brings together the RISC-V core IP integration and SoC design verification, as well as a full-featured reference design kit consisting of real-time operating system (RTOS) and peripherals drivers, all on a 55nm process for battery-powered edge devices. This highlights how the hardware manufacturers can differentiate around a standard ISA. Faraday has included dynamic voltage and frequency scaling (DVFS), power mode switching and fast system wake-up in the platform, but can safely include the software libraries and drivers to ensure the chips work seamlessly for specific interfacing, sensing and power-management functions.

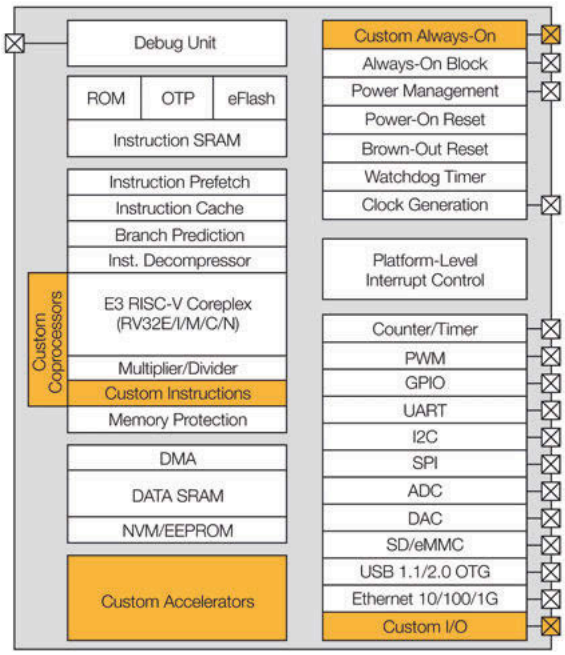
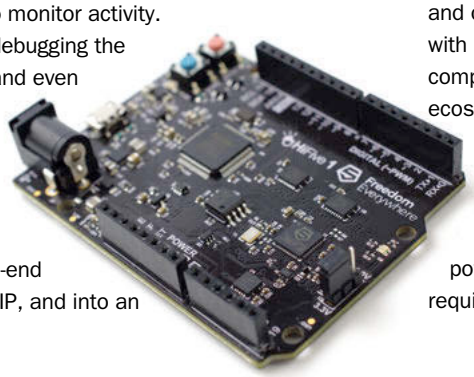


Figure 2: The E300 series of open-source 32-bit microcontrollers using the RISC-V ISA

RISC-V ISA can also be used with a wide range of tools. Microsemi has used the ISA across its FPGAs with a range of embedded operating systems such as Express Logic's ThreadX, Huawei LiteOS and Micrium µC/OS-II. Boards include the RTG4 development kit, the PolarFire evaluation kit, etc. Debug dongles from Microsemi and Olimex, first-stage bootloaders and multiple soft peripherals are also included. Examples of drivers, firmware and projects are available on GitHub.

Another tool company benefiting from its stability is UltraSoC, which develops hardware that can be embedded in a SoC to monitor activity. This can be used for debugging the chip more effectively and even used in the field for monitoring. It has been working with Andes on integrating the monitoring hardware into the high-end AndesCore processor IP, and into an AI "supercomputer-on-a-chip" from Esperanto Technologies that uses thousands of RISC-V cores.

Figure 3: The HiFive1 RISC-V development kit



RISC-V challenges

Though considerable headway has already been made in relation to RISC-V's development and proliferation, there are obstacles ahead. Researchers at Princeton University have uncovered a number of flaws in the RISC-V open-source processor core that they believe to be significant. They found more than 100 errors involving incorrect ordering of the storage and retrieval of information from memory in variations of the RISC-V processor architecture that, if uncorrected, could cause issues in software running on RISC-V chips.

The RISC-V Foundation said the errors would not affect most versions of RISC-V, but might have been more problematic for higher-performance systems.

With a common, frozen ISA across 32-bit, 64-bit and even 128-bit (when they emerge) address spaces, core developers can focus on the particular processor implementations, whether for research projects, IoT nodes or a supercomputer-on-a-chip. All these use the same compilers, the same development tools and the same debug tools, minimising fragmentation and allowing companies to keep pushing performance benchmarks rather than worrying about maintenance of multiple software products for multiple cores – and all, of course, with an open-source ethos that allows improvements to be fed back into the industry.

Extensions allow for differentiation and optimisation, particularly with regard to security, without compromising the stability of the tool ecosystem.

In this way, RISC-V allows hardware developers to focus on innovation, driven by the software needs to meet the cost, power, security and performance requirements of end users.

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A TOUCH-FREE WORLD

Optical sensors are being used to help create a safer, touch-free world as a result of COVID, as **Gabriele Fulco** explains to New Electronics

Contactless sensors are proving their worth, as the coronavirus crisis focuses attention on the need to count numbers of people in spaces, even to measure the temperature of individual humans within their field of vision.

No-contact sensors provide the solid basis to solutions for access control and body temperature measurement – both of which provide countermeasures to the Covid-19 threat – and recent developments, have made these vital devices more dependable and reliable. Such sensors can also replace 'touch-based' switches to operate lights and other services, eliminating a further potential infection vector.

Automated access control facilitates the distancing required for effective infection control within buildings, rooms and even crowd-controlled open spaces, while temperature measurements can detect the presence or absence of people, or to confirm that a system is operational.

For all these situations, thermal sensors represent a well-established option where the application calls simply for the detection of people. More pertinently, accurate human temperature monitoring will alert building operators to a fever and potential Covid-19 infection amongst those seeking to gain access.

Such sensors need a wide field of view, so that they can detect the presence and location of people, and other issues in a space, accurately and reliably. The Omron D6T thermal sensor, for example, is based on an infrared sensor which measures the surface temperature of objects without touching them. It does this by using a thermopile element, which absorbs radiated energy from the target object.

The MEMS thermopile is integrated with a custom designed sensor ASIC that bundles a signal processing microprocessor and algorithm into a tiny package. As a result, the sensor is said to offer the highest signal-to-noise ratio (SNR) in the industry. Clear and reliable measurements can easily be interpreted by the system.

Figure 1: A matrix type of sensor such as Omron's D6T 4x4 makes it easy to separate human and background temperatures.

Separating people from the background

A matrix type of sensor makes it easy to separate human and background temperatures (Figure 1). Practical applications therefore depend on the number of sensor elements and how close the array is to the human. Using infrared detectors means there is no attenuation of signals by the atmosphere, so resolution depends entirely on the sensor's field of view (FOV).

Many such applications can be served by established products, ranging from a single sensor element, up to arrays of 1024 elements. The D6T 4x4 sensor can measure face temperature at distances up to 1m for access control, whilst the D6T single-eye sensor is more suitable for wrist or forehead wearable devices. With suitable calibration, temperature accuracy on the D6T 4x4 sensor can reach ±0.2°C giving a reliable identification of fever.

At longer distances, the wide-angle version of the device based on 32 x 32 elements provides a view across 90.0° by 90.0° (Figure 2). This equates to a square field of view measuring 200cm x 200cm, so allows people to be detected in a whole room from a single point. In this case, reduced precision makes fever detection somewhat unreliable at long distances. Nevertheless, it is accurate where the target is 100cm away, and it is even possible to make reliable temperature measurements where the face is partially obscured, for example by glasses, goggles or a PPE face mask.

Reducing COVID infection

Dealing with a pandemic requires more than just data. Intelligence in the form of human vision technology adds a further dimension to coronavirus countermeasures based on optical sensors. Smart optical sensors such as HVC-2 image sensors (Figure 3), can detect faces, facial features and human bodies – even estimating age and gender of the humans in the captured images.

Any embedded developer can add face recognition functionality to a system without the need to understand the algorithms or the optical design. This in turn makes it possible, for example, to link with databases for tracing coronavirus victims and tracking their contacts.

Human Vision Components are modular solutions, and each provides

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ten key image sensing functions: detection of a human face, hand or body, face recognition, gender detection, age estimation, mood estimation, facial pose estimation, gaze estimation and blink estimation. In each case, the module returns a value together with a degree of certainty, allowing programmers to configure the response appropriately for each individual application. No personal or private data are stored, so these devices do not compromise the subject's privacy.

The technology comes in a very compact configuration. It can be readily integrated into established systems or implemented as part of a new design.

Basic sensing functions could aid distancing in the workplace or public spaces by counting the number of people in the room or detecting when people are too close together. More sophisticated solutions – for example applied to digital signage, vending machines and payment stations - will help eliminate the need for physical human contact. One example: automatic face detection, age estimation and gender estimation could reduce the amount of physical interaction for customers who stand in front of the digital signage. Such an approach could be used identify people in at-risk categories and present them with specially targeted messages.

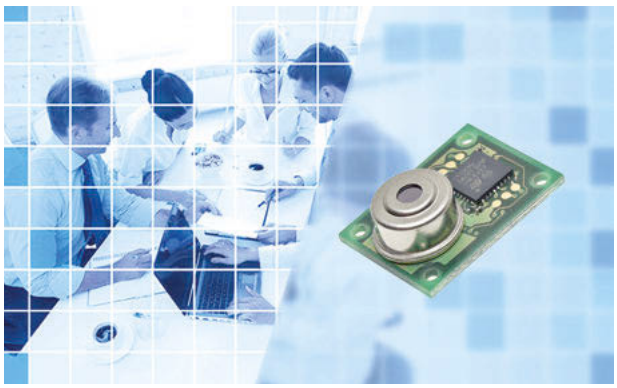

Figure 2: Omron D6T 32x32 has a large field of view allowing people to be detected in a whole room from a single point.

Using these sensors, a variety of infection-limiting precautions could be integrated together using one set of vision modules. The data they collect can be responded to automatically, saved or collated centrally, and passed to an operator only when necessary. Applied to workplaces, it could track individuals through the premises, recognising when arrive and leave, and reducing physical contact by setting-up heating, ventilation and lighting to individual requirements.

The range of applications extends beyond public spaces and the workplace. Medical and care facilities are another sector where image sensors can help in the fight against Covid-19. From access control based on body temperature or facial recognition, the image sensor can help maintain distancing and reduce overcrowding, additionally separating the infected from the healthy.

Figure 3: Smart optical sensors such as Omron's HVC-2 image sensors can even estimate age and gender of the humans in the captured images.

Contactless switching

Pre-COVID, we all reached for the light switch in a room without a second thought, but these days we are more cautious. Doors, drinks dispensers, soap dispensers, toilet flushes – every day in the workplace and other public environments we touch countless switches that have also been touched by hundreds of complete strangers. This is no longer acceptable to many, and may indeed become the subject of regulatory restrictions. Fortunately, contactless sensors provide an ideal solution that can easily be implemented in environments where the spread of harmful bacteria and viruses needs to be reduced. The latest devices offer exceptional performance, with a longer detection distance and a convergent light beam that triggers accurately on an object within a tightly specified target area, ignoring any objects in the background or foreground.

Omron B5W-LB LCR sensors are reliable and offer repeatability of their detection performance, even when presented with target items of different colours and types of surface including reflective surfaces. With digital outputs, designers are offered a simple and easy to integrated electronic control that reliably delivers the expected performance.

Who knows what the 'new normal' will actually look like? Without a doubt though, there is a real need for changes to the workplace and the home in the light of our recent experience.

Opto-sensing technology has an important part to play, and it may well be that contactless switches will become the norm even when COVID is a distant memory.

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Lattice Radiant Software Tool Accelerates System Development for New Certus-NX FPGA-based Designs

Easy-to-Use, Best-in-Class FPGA Design Tool Also Supports SystemVerilog

Lattice Semiconductor Corporation (NASDAQ: LSCC), the low power programmable leader, today announced availability of the latest version of its popular software design tool for FPGAs, Lattice Radiant™ 2.1. The version includes support for the company's new general-purpose Lattice Certus™-NX FPGAs, the second family introduced within six months using Lattice Nexus™ FPGA development platform, plus native support for the SystemVerilog hardware description and verification language to increase functionality and design flexibility. Lattice Radiant design software accelerates development of Lattice FPGA-based applications for a range of markets, including industrial/automotive, communications/compute, and consumer.

The new version of Radiant supports SystemVerilog throughout the entire design flow, from the native synthesis tool through the schematic viewer, hierarchical viewer, configuration wizards, and debugging tool. This highly productive coding method simplifies on-chip debugging and other tasks to streamline the design process and get Lattice FPGA-based products to market faster. Lattice has made Radiant even easier to use as the tool's drag-and-drop GUI has been redesigned with support for an I/O planner that enforces correct pin placement for each I/O signal or bus.

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New Switch'Air™ Domes with Hole from Nicomatic

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New Switch'Air™ Domes with Hole from Nicomatic enable integration of LEDs into electrical membrane switches and eliminate suction effect for faster, easier automatic assembly

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Nicomatic, the leading manufacturer of high performance interconnect systems, has added new Switch'Air™ Domes with Hole to its successful Switch'Air 4-legged Domes range. Switch'Air™ Domes feature patented technology with a cushion of air that prevents domes sticking to each other during automated pick & place manufacturing, resulting in faster, easier, more accurate assembly. With a life expectancy of up to five million actuations and guaranteed for one million actuation cycles, Switch'Air domes provide reliable, extended-life performance for demanding applications in the medical and industrial markets among others.

New Switch'Air Domes with Hole are specifically designed for membrane switches, sitting free in the spacer layer of the membrane.

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Nexperia announces next generation 650 V Gallium Nitride Technology

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Next-gen GaN technology targets automotive, 5G and datacenter applications; Devices available packaged in TO-247 and innovative Copper Clip SMD

Nexperia, the expert in essential semiconductors, has announced a new range of GaN FET devices featuring next-gen high-voltage GaN HEMT H2 technology in both TO-247 and the company's proprietary CCPAK surface mount packaging. Devices achieve superior switching FOMs and on-state performance with improved stability, and simplify application designs thanks to their cascode configuration which eliminates the need for complicated drivers and controls.

The new GaN technology employs through-epi vias, reducing defects and shrinking die size by around 24%. RDS(on) is also reduced to just 41 mΩ (max., 35 mΩ typ. at 25 °C) with the initial release in traditional TO-247, with high threshold voltage and low diode forward voltage. The reduction will further increase, to 39 mΩ (max., 33 mΩ typ. At 25 °C) with CCPAK surface-mount versions. Because the parts are configured as cascode devices, they are also simple to drive using standard Si MOSFET drivers. Both versions meet the demands of AEC-Q101 for automotive applications.

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Pickering Electronics' miniature HV reed relay at the heart of IC test system

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Pickering Electronics' miniature HV reed relay at the heart of IC test system for On Semiconductor

Custom request becomes industry's smallest high voltage reed relay

Pickering Electronics, the reed relay company which has pioneered miniaturization and high performance for over 50 years, has announced that it has developed a miniature high voltage relay for use in a new test rig, designed by globally-renowned chip maker, ON Semiconductor.

In switching systems for test and measurement applications, reed relays are often the best solution thanks to their small size, high isolation resistance, hermetically sealed contacts, fast operate time and long-life expectancy. When developing a new test rig, ON Semiconductor – a long-standing customer of Pickering - identified the need for a reed relay with a stand-off voltage of at least 400VDC, which was also small enough to meet its demanding high switching density requirements.

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Pickering Interfaces launches turnkey LXI microwave switch

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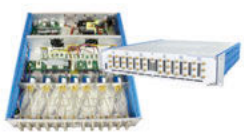
Pickering Interfaces launches turnkey LXI microwave switch and signal routing subsystem service



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The service provides compact, rack-mounted, multiplexer, matrix and complex routing designs based on an industry-standard LXI/Ethernet interface, designed and manufactured by Pickering's team of switching experts. Solutions are available with bandwidths from DC to 67 GHz @ 50Ω, with terminated or unterminated options and bandwidths up to 2.5 GHz @ 75Ω.

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Power Integrations Releases Highly Integrated InnoSwitch3

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Power Integrations Releases Highly Integrated InnoSwitch3 Flyback Switcher IC for Automotive BEV and PHEV Applications

InnoSwitch3-AQ achieves Q100; operates efficiently from 30 V to 550 V DC input

Power Integrations (Nasdaq: POWI), the leader in high-voltage integrated circuits for energy-efficient power conversion, today announced the production release of the InnoSwitch™3-AQ, an AEC-Q100-qualified flyback switcher with integrated 750 V MOSFET and secondary-side sensing. The newly qualified device family targets automotive EV applications, such as traction inverter, OBC (on-board charger), EMS (energy management DC/DC bus converters) and BMS (battery management systems).

The InnoSwitch3-AQ uses Power Integrations' high-speed FluxLink™ coupling to achieve ±3% accuracy for combined line and load regulation while eliminating both dedicated isolated transformer sense-windings and optocouplers. FluxLink technology maintains output voltage regulation even under the transient stress test, which is particularly challenging for PSR-based implementations.

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Smiths Interconnect celebrates significant contract win with Boeing

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Docking connectors will ensure consistent connection on NASA's Orion spacecraft and Lunar Gateway

Smiths Interconnect was recently awarded a contract by Boeing to design, manufacture and supply bespoke connectors for use aboard NASA's Orion spacecraft and Lunar Gateway.

Smiths Interconnect's docking umbilical connectors will be used to transfer power, signal and communications to different modules on the space station.

"These connectors have to meet strict specifications to endure the challenges of space. They must deliver high speed signal integrity to ensure there is a strong, consistent connection throughout the mission," said Paul Harris, VP Sales and Marketing at Smiths Interconnect. "With many phases of the Artemis programme still to come, we hope that our partnership with Boeing will stretch many decades as we explore Mars and the wonders that the planet has to offer."

The Orion spacecraft will take up to four astronauts to the Lunar Gateway where they will board a human landing system for exploration missions to the surface of the Moon.

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